Application Report
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Fundamentals of MOSFET and IGBT Gate Driver Circuits

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ABSTRACT

The main purpose of this application report is to demonstrate a systematic approach to design high performance gate drive circuits for high speed switching applications. It is an informative collection of topics offering a “one-stop-shopping” to solve the most common design challenges. Therefore, it should be of interest to power electronics engineers at all levels of experience.

The most popular circuit solutions and their performance are analyzed, including the effect of parasitic components, transient and extreme operating conditions. The discussion builds from simple to more complex problems starting with an overview of MOSFET technology and switching operation. Design procedure for ground referenced and high side gate drive circuits, AC coupled and transformer isolated solutions are described in great details. A special section deals with the gate drive requirements of the MOSFETs in synchronous rectifier applications. For more information, see the Overview for MOSFET and IGBT Gate Drivers product page.

Several, step-by-step numerical design examples complement the application report.

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1 Introduction

MOSFET – is an acronym for Metal Oxide Semiconductor Field Effect Transistor and it is the key component in high frequency, high efficiency switching applications across the electronics industry. It might be surprising, but FET technology was invented in 1930, some 20 years before the bipolar transistor. The first signal level FET transistors were built in the late 1950's while power MOSFETs have been available from the mid 70's. Today, millions of MOSFET transistors are integrated in modern electronic components, from microprocessors, through "discrete" power transistors.

The focus of this topic is the gate drive requirements of the power MOSFET in various switch mode power conversion applications.

2 MOSFET Technology

The bipolar and the MOSFET transistors exploit the same operating principle. Fundamentally, both type of transistors are charge controlled devices, which means that their output current is proportional to the charge established in the semiconductor by the control electrode. When these devices are used as switches, both must be driven from a low impedance source capable of sourcing and sinking sufficient current to provide for fast insertion and extraction of the controlling charge. From this point of view, the MOSFETs have to be driven just as "hard" during turn-on and turn-off as a bipolar transistor to achieve comparable switching speeds. Theoretically, the switching speeds of the bipolar and MOSFET devices are close to identical, determined by the time required for the charge carriers to travel across the semiconductor region. Typical values in power devices are approximately 20 to 200 picoseconds depending on the size of the device.

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The popularity and proliferation of MOSFET technology for digital and power applications is driven by two of their major advantages over the bipolar junction transistors. One of these benefits is the ease of use of the MOSFET devices in high frequency switching applications. The MOSFET transistors are simpler to drive because their control electrode is isolated from the current conducting silicon, therefore a continuous ON current is not required. Once the MOSFET transistors are turned-on, their drive current is practically zero. Also, the controlling charge and accordingly the storage time in the MOSFET transistors is greatly reduced. This basically eliminates the design trade-off between on state voltage drop, which is inversely proportional to excess control charge, and turn-off time. As a result, MOSFET technology promises to use much simpler and more efficient drive circuits with significant economic benefits compared to bipolar devices.

Furthermore, it is especially important to highlight for power applications, that MOSFETs have a resistive nature. The voltage drop across the drain source terminals of a MOSFET is a linear function of the current flowing in the semiconductor. This linear relationship is characterized by the $R_{DS(on)}$ of the MOSFET and known as the on-resistance. On-resistance is constant for a given gate-to-source voltage and temperature of the device. As opposed to the -2.2mV/°C temperature coefficient of a p-n junction, the MOSFETs exhibit a positive temperature coefficient of approximately 0.7%/°C to 1%/°C. This positive temperature coefficient of the MOSFET makes it an ideal candidate for parallel operation in higher power applications where using a single device would not be practical or possible. Due to the positive TC of the channel resistance, parallel connected MOSFETs tend to share the current evenly among themselves. This current sharing works automatically in MOSFETs since the positive TC acts as a slow negative feedback system. The device carrying a higher current will heat up more – don't forget that the drain to source voltages are equal – and the higher temperature will increase its $R_{DS(on)}$ value. The increasing resistance will cause the current to decrease, therefore the temperature to drop. Eventually, an equilibrium is reached where the parallel connected devices carry similar current levels. Initial tolerance in $R_{DS(on)}$ values and different junction to ambient thermal resistances can cause significant – up to 30% – error in current distribution.

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2.1 Device Types

Almost all manufacturers have their unique twist on how to manufacture the best power MOSFETs, but all of these devices on the market can be categorized into three basic device types. These are illustrated in Figure 1.

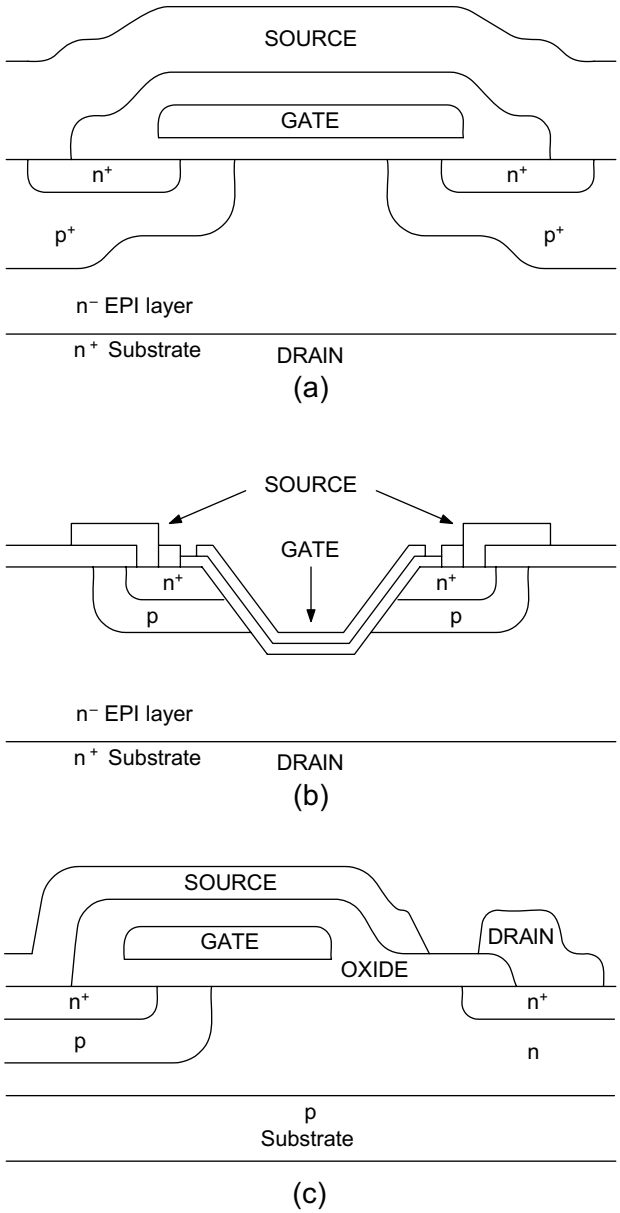

Figure 1. Power MOSFET Device Types

Double-diffused MOS transistors were introduced in the 1970's for power applications and evolved continuously during the years. Using polycrystalline silicon gate structures and self-aligning processes, higher density integration and rapid reduction in capacitances became possible.

The next significant advancement was offered by the V-groove or trench technology to further increase cell density in power MOSFET devices. The better performance and denser integration do not come free; however, as trench MOS devices are more difficult to manufacture.

The lateral power MOSFETs have significantly lower capacitances, therefore, they can switch much faster and they require much less gate drive power.

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2.2 MOSFET Models

There are numerous models available to illustrate how the MOSFET works, nevertheless finding the right representation might be difficult. Most of the MOSFET manufacturers provide Spice and/or Saber models for their devices, but these models say very little about the application traps designers have to face in practice. They provide even fewer clues how to solve the most common design challenges.

A really useful MOSFET model that describes all important properties of the device from an application point of view would be very complicated. On the other hand, very simple and meaningful models can be derived of the MOSFET transistor if we limit the applicability of the model to certain problem areas.

The first model in Figure 2 is based on the actual structure of the MOSFET device and can be used mainly for DC analysis. The MOSFET symbol in Figure 2a represents the channel resistance and the JFET corresponds to the resistance of the epitaxial layer. The length, therefore, the resistance of the epi layer is a function of the voltage rating of the device as high voltage MOSFETs require thicker epitaxial layer.

Figure 2b can be used very effectively to model the dv/dt induced breakdown characteristic of a MOSFET. It shows both main breakdown mechanisms, namely the dv/dt induced turn-on of the parasitic bipolar transistor present in all power MOSFETs and the dv/dt induced turn-on of the channel, as a function of the gate terminating impedance. Modern power MOSFETs are practically immune to dv/dt triggering of the parasitic npn transistor due to manufacturing improvements to reduce the resistance between the base and emitter regions.

It must be mentioned also that the parasitic bipolar transistor plays another important role. Its base – collector junction is the famous body diode of the MOSFET.

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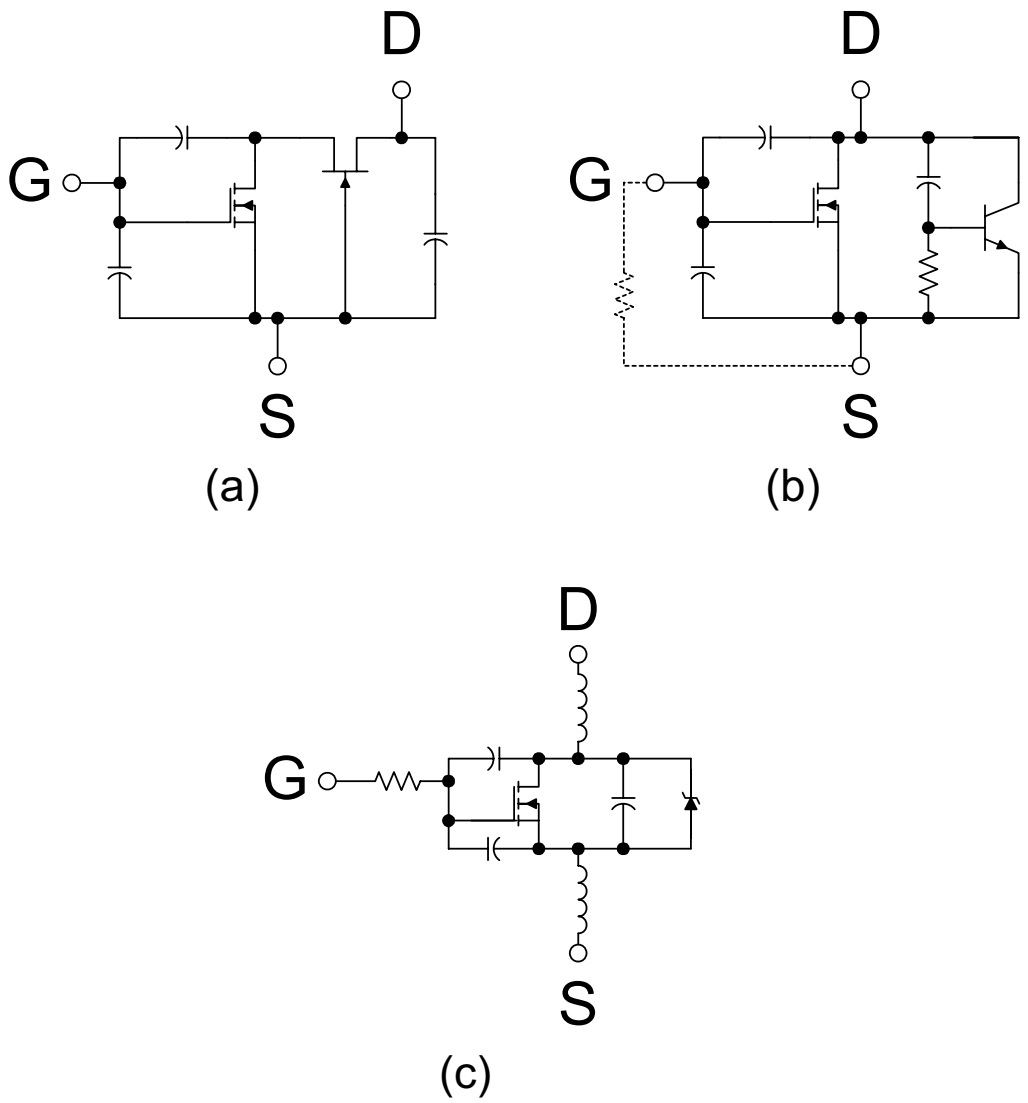

Figure 2. Power MOSFET Models

Figure 2c is the switching model of the MOSFET. The most important parasitic components that influences switching performance are shown in this model. Their respective roles are discussed in Section 2.3, which is dedicated to the switching procedure of the device.

2.3 MOSFET Critical Parameters

When switch mode operation of the MOSFET is considered, the goal is to switch between the lowest and highest resistance states of the device in the shortest possible time. Since the practical switching times of the MOSFETs (approximately 10 ns to 60 ns) is at least two to three orders of magnitude longer than the theoretical switching time (approximately 50 ps to 200 ps), it seems important to understand the discrepancy. Referring back to the MOSFET models in Figure 2, note that all models include three capacitors connected between the three terminals of the device. Ultimately, the switching performance of the MOSFET transistor is determined by how quickly the voltages can be changed across these capacitors.

Therefore, in high speed switching applications, the most important parameters are the parasitic capacitances of the device. Two of these capacitors, the C_{GS} and C_{GD} capacitors correspond to the actual geometry of the device while the C_{DS} capacitor is the capacitance of the base collector diode of the parasitic bipolar transistor (body diode).

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The C_{GS} capacitor is formed by the overlap of the source and channel region by the gate electrode. Its value is defined by the actual geometry of the regions and stays constant (linear) under different operating conditions.

The C_{GD} capacitor is the result of two effects. Part of it is the overlap of the JFET region and the gate electrode in addition to the capacitance of the depletion region, which is non-linear. The equivalent C_{GD} capacitance is a function of the drain source voltage of the device approximated by Equation 1.

$$C_{GD} \approx \frac{C_{GD,0}}{1 + K_1 \times \sqrt{V_{DS}}} \tag{1}$$

The C_{DS} capacitor is also non-linear since it is the junction capacitance of the body diode. Its voltage dependence can be described as shown in Equation 2.

$$C_{DS} \approx \frac{C_{DS,0}}{K_2 \times \sqrt{V_{DS}}} \tag{2}$$

Unfortunately, non of the above mentioned capacitance values are defined directly in the transistor data sheets. Their values are given indirectly by the C_{ISS}, C_{RSS}, and C_{OSS} capacitor values and must be calculated as shown in Equation 3:

$$C_{GD} = C_{RSS}$$

$$C_{GS} = C_{ISS} - C_{RSS}$$

$$C_{DS} = C_{OSS} - C_{RSS} \tag{3}$$

Further complication is caused by the C_{GD} capacitor in switching applications because it is placed in the feedback path between the input and output of the device. Accordingly, its effective value in switching applications can be much larger depending on the drain source voltage of the MOSFET. This phenomenon is called the “Miller” effect and it can be expressed as shown in Equation 4.

$$C_{GD,eqv} = (1 + g_{fs} \times R_L) \times C_{GD} \tag{4}$$

Since the C_{GD} and C_{DS} capacitors are voltage dependent, the data sheet numbers are valid only at the test conditions listed. The relevant average capacitances for a certain application have to be calculated based on the required charge to establish the actual voltage change across the capacitors. For most power MOSFETs the approximations shown in Equation 5.

$$C_{GD,ave} = 2 \times C_{RSS,spec} \times \sqrt{\frac{V_{DS,spec}}{V_{DS,off}}}$$

$$C_{OSS,ave} = 2 \times C_{OSS,spec} \times \sqrt{\frac{V_{DS,spec}}{V_{DS,off}}} \tag{5}$$

The next important parameter to mention is the gate mesh resistance, $R_{G,I}$. This parasitic resistance describes the resistance associated by the gate signal distribution within the device. Its importance is very significant in high speed switching applications because it is in between the driver and the input capacitor of the device, directly impeding the switching times and the dv/dt immunity of the MOSFET. This effect is recognized in the industry, whereas, real high speed devices like RF MOSFET transistors use metal gate electrodes instead of the higher resistance polysilicon gate mesh for gate signal distribution. The $R_{G,I}$ resistance is not specified in the data sheets, but in certain applications it can be a very important characteristic of the device. Appendix A4 shows a typical measurement setup to determine the internal gate resistor value with an impedance bridge.

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Obviously, the gate threshold voltage is also a critical characteristic. It is important to note that the data sheet V_{TH} value is defined at 25°C and at a very low current, typically at 250 μA. Therefore, it is not equal to the Miller plateau region of the commonly known gate switching waveform. Another rarely mentioned fact about V_{TH} is its approximately –7 mV/°C temperature coefficient. It has particular significance in gate drive circuits designed for logic level MOSFET where V_{TH} is already low under the usual test conditions. Since MOSFETs usually operate at elevated temperatures, proper gate drive design must account for the lower V_{TH} when turn-off time, and dv/dt immunity is calculated as shown in Seminar 1400 Topic 2 Appendix A/F Est MOSFET Parameters from the Data Sheet.

The transconductance of the MOSFET is its small signal gain in the linear region of its operation. It is important to point out that every time the MOSFET is turned-on or turned-off, it must go through its linear operating mode where the current is determined by the gate-to-source voltage. The transconductance, g_{fs}, is the small signal relationship between drain current and gate-to-source voltage as shown in Equation 6.

$$g_{fs} = \frac{dI_D}{dV_{GS}} \tag{6}$$

Accordingly, the maximum current of the MOSFET in the linear region is shown in Equation 7.

$$I_D = (V_{GS} - V_{th}) \times g_{fs} \tag{7}$$

Rearranging this equation for V_{GS} yields the approximate value of the Miller plateau as a function of the drain current as shown in Equation 8.

$$V_{GS,Miller} = V_{th} + \frac{I_D}{g_{fs}} \tag{8}$$

Other important parameters like the source inductance (L_S) and drain inductance (L_D) exhibit significant restrictions in switching performance. Typical LS and LD values are listed in the data sheets, and they are mainly dependant on the package type of the transistor. Their effects can be investigated together with the external parasitic components usually associated with layout and with accompanying external circuit elements like leakage inductance, a current sense resistor, and so forth.

For completeness, the external series gate resistor and the MOSFET driver's output impedance must be mentioned as determining factors in high performance gate drive designs as they have a profound effect on switching speeds and consequently on switching losses.

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2.4 Switching Applications

Now, that all the players are identified, the actual switching behavior of the MOSFET transistors needs to be investigated. To gain a better understanding of the fundamental procedure, the parasitic inductances of the circuit will be neglected. Later their respective effects on the basic operation will be analyzed individually. Furthermore, the following descriptions relate to clamped inductive switching because most MOSFET transistors and high speed gate drive circuits used in switch mode power supplies work in that operating mode.

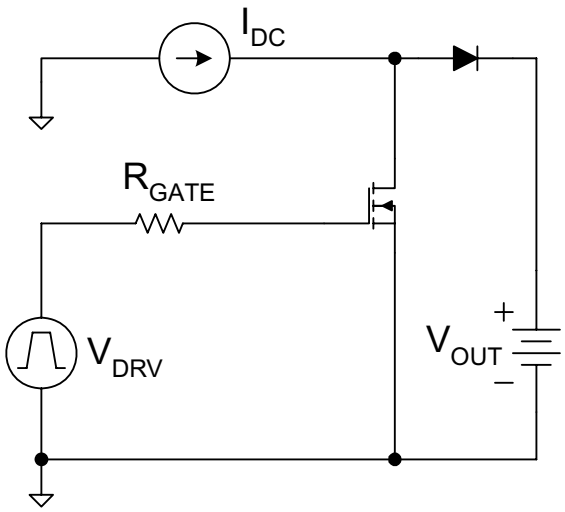

Figure 3. Simplified Clamped Inductive Switching Model

The simplest model of clamped inductive switching is shown in Figure 3, where the DC current source represents the inductor. Its current can be considered constant during the short switching interval. The diode provides a path for the current during the off time of the MOSFET and clamps the drain terminal of the device to the output voltage symbolized by the battery.

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2.5 Turn-On Procedure

The turn-on event of the MOSFET transistor can be divided into four intervals as depicted in Figure 4.

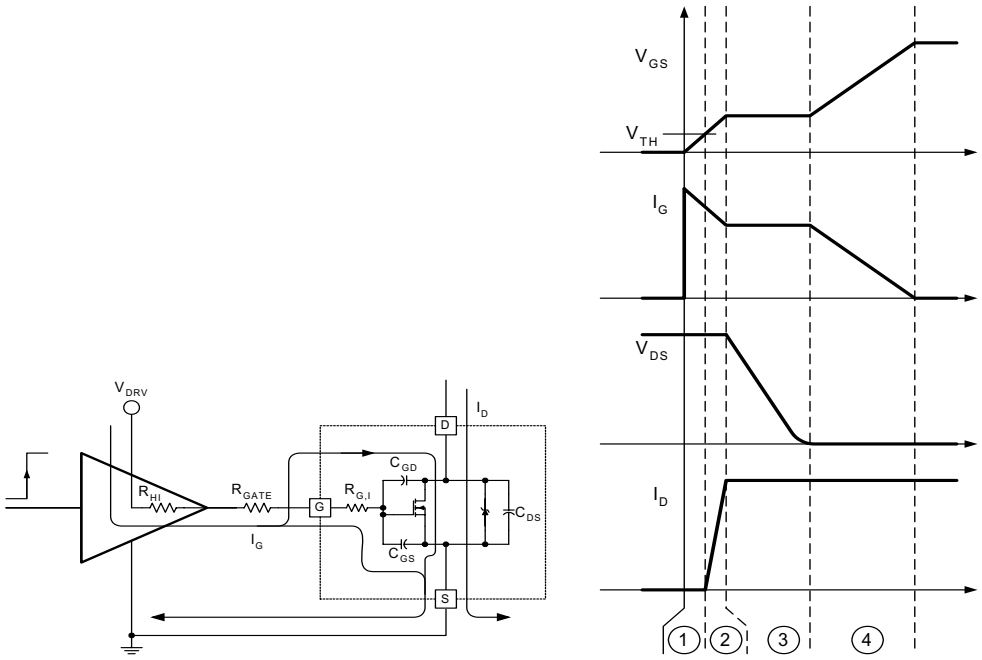

Figure 4. MOSFET Turn-On Time Intervals

In the first step, the input capacitance of the device is charged from 0 V to V_{TH}. During this interval most of the gate current is charging the C_{GS} capacitor. A small current is flowing through the C_{GD} capacitor, too. As the voltage increases at the gate terminal and the C_{GD} capacitor's voltage has to be slightly reduced. This period is called the turn-on delay, because both the drain current and the drain voltage of the device remain unchanged.

Once the gate is charged to the threshold level, the MOSFET is ready to carry current. In the second interval, the gate is rising from V_{TH} to the Miller plateau level, $V_{GS,Miller}$. This is the linear operation of the device when current is proportional to the gate voltage. On the gate side, current is flowing into the C_{GS} and C_{GD} capacitors just like in the first time interval and the V_{GS} voltage is increasing. On the output side of the device, the drain current is increasing, while the drain-to-source voltage stays at the previous level ($V_{DS,off}$). This can be understood looking at the schematic in Figure 3. Until all the current is transferred into the MOSFET and the diode is turned-off completely to be able to block reverse voltage across its pn junction, the drain voltage must stay at the output voltage level.

Entering into the third period of the turn-on procedure the gate is already charged to the sufficient voltage ($V_{GS,Miller}$) to carry the entire load current and the rectifier diode is turned off. That now allows the drain voltage to fall. While the drain voltage falls across the device, the gateto- source voltage stays steady. This is the Miller plateau region in the gate voltage waveform. All the gate current available from the driver is diverted to discharge the C_{GD} capacitor to facilitate the rapid voltage change across the drain-to-source terminals. The drain current of the device stays constant since it is now limited by the external circuitry, that is, the DC current source.

The last step of the turn-on is to fully enhance the conducting channel of the MOSFET by applying a higher gate drive voltage. The final amplitude of V_{GS} determines the ultimate on-resistance of the device during its on-time. Therefore, in this fourth interval, V_{GS} is increased from $V_{GS,Miller}$ to its final value, V_{DRV}. This is accomplished by charging the C_{GS} and C_{GD} capacitors, thus gate current is now split between the two components. While these capacitors are being charged, the drain current is still constant, and the drain-to-source voltage is slightly decreasing as the on resistance of the device is being reduced.

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2.6 Turn-Off Procedure

The description of the turn-off procedure for the MOSFET transistor is basically back tracking the turn-on steps from the previous section. Start with V_{GS} being equal to V_{DRV} and the current in the device is the full load current represented by IDC in Figure 3. The drain-to-source voltage is being defined by IDC and the $R_{DS(on)}$ of the MOSFET. The four turn-off steps are shown in Figure 5. for completeness.

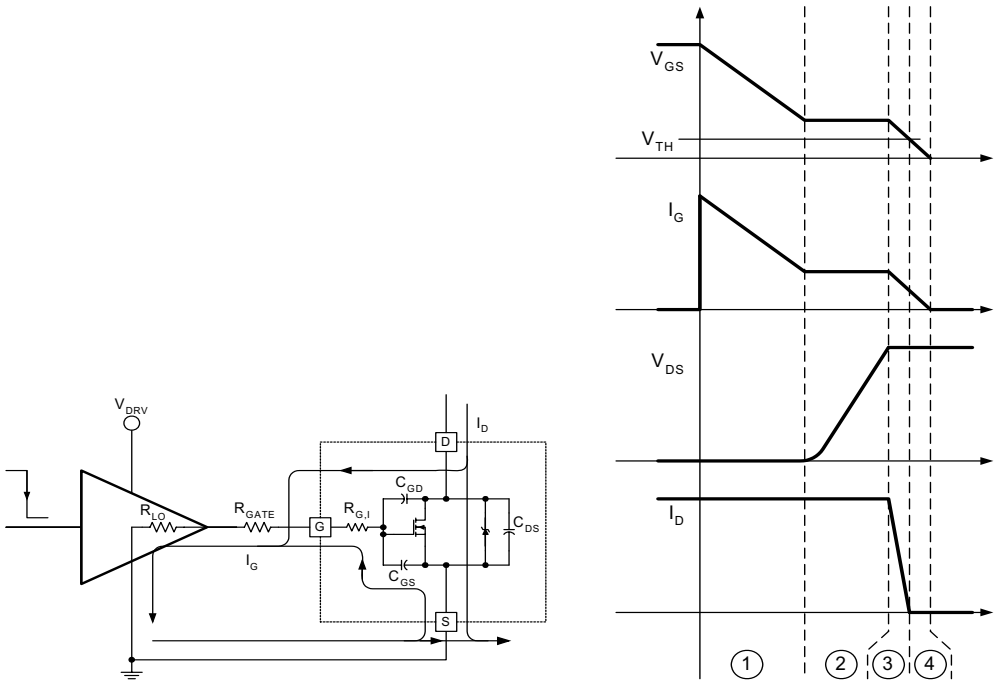

Figure 5. MOSFET Turn-Off Time Intervals

The first time interval is the turn-off delay that is required to discharge the C_{ISS} capacitance from its initial value to the Miller plateau level. During this time, the gate current is supplied by the C_{ISS} capacitor itself and it is flowing through the C_{GS} and C_{GD} capacitors of the MOSFET. The drain voltage of the device is slightly increasing as the overdrive voltage is diminishing. The current in the drain is unchanged.

In the second period, the drain-to-source voltage of the MOSFET rises from $ID \cdot R_{DS(on)}$ to the final $V_{DS,off}$ level, where it is clamped to the output voltage by the rectifier diode according to the simplified schematic of Figure 3. During this time period, which corresponds to the Miller plateau in the gate voltage waveform, the gate current is strictly the charging current of the C_{GD} capacitor because the gate-to-source voltage is constant. This current is provided by the bypass capacitor of the power stage and it is subtracted from the drain current. The total drain current still equals the load current, that is, the inductor current represented by the DC current source in Figure 3.

The beginning of the third time interval is signified by the turn-on of the diode, thus providing an alternative route to the load current. The gate voltage resumes falling from $V_{GS,Miller}$ to V_{TH}. The majority of the gate current is coming out of the C_{GS} capacitor, because the C_{GD} capacitor is virtually fully charged from the previous time interval. The MOSFET is in linear operation and the declining gate-to-source voltage causes the drain current to decrease and reach near zero by the end of this interval. Meanwhile the drain voltage is steady at $V_{DS,off}$ due to the forward biased rectifier diode.

The last step of the turn-off procedure is to fully discharge the input capacitors of the device. V_{GS} is further reduced until it reaches 0 V. The bigger portion of the gate current, similarly to the third turn-off time interval, supplied by the C_{GS} capacitor. The drain current and the drain voltage in the device are unchanged.

Summarizing the results, it can be concluded that the MOSFET transistor can be switched between its highest and lowest impedance states (either, turn-on or turn-off) in four time intervals. The lengths of all four time intervals are a function of the parasitic capacitance values, the required voltage change across them and the available gate drive current. This emphasizes the importance of the proper component selection and optimum gate drive design for high speed, high frequency switching applications.

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Unfortunately, these numbers correspond to the specific test conditions and to resistive loads, making the comparison of different manufacturers' products difficult. Also, switching performance in practical applications with clamped inductive load is significantly different from the numbers given in the data sheets.

2.7 Power Losses

The switching action in the MOSFET transistor in power applications results in some unavoidable losses, which can be divided into two categories.

The simpler of the two loss mechanisms is the gate drive loss of the device. As described before, turning-on or off the MOSFET involves charging or discharging the C_{ISS} capacitor. When the voltage across a capacitor is changing, a certain amount of charge has to be transferred. The amount of charge required to change the gate voltage between 0 V and the actual gate drive voltage V_{DRV}, is characterized by the typical gate charge vs. gate-to-source voltage curve as shown in Figure 6.

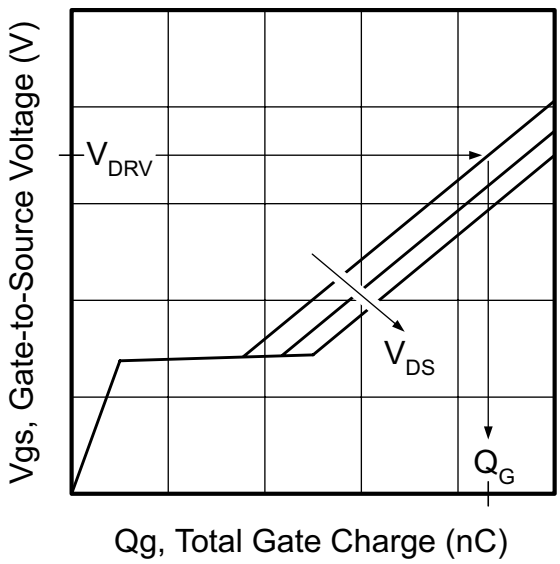

Figure 6. Typical Gate Charge vs. Gate-to-Source Voltage

This graph gives a relatively accurate worst case estimate of the gate charge as a function of the gate drive voltage. The parameter used to generate the individual curves is the drain-tosource off state voltage of the device. $V_{DS,off}$ influences the Miller charge – the area below the flat portion of the curves – thus also, the total gate charge required in a switching cycle. Once the total gate charge is obtained from Figure 6, the gate charge losses can be calculated as shown in Equation 9.

$$PGATE = V_{DRV} \times QG \times f_{DRV}$$

where

- V_{DRV} is the amplitude of the gate drive waveform
- f_{DRV} is the gate-drive frequency, in most cases equal to the switching frequency (9)

It is interesting to notice that the $Q_G \cdot f_{DRV}$ term in the previous equation gives the average bias current required to drive the gate.

The power lost to drive the gate of the MOSFET transistor is dissipated in the gate drive circuitry. Referring back to Figure 4 and Figure 5, the dissipating components can be identified as the combination of the series ohmic impedances in the gate drive path. In every switching cycle the required gate charge has to pass through the driver output impedances, the external gate resistor, and the internal gate mesh resistance. As it turns out, the power dissipation is independent of how quickly the charge is delivered through the resistors.

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Using the resistor designators from Figure 4 and Figure 5, the driver power dissipation can be expressed as shown in Equation 10.

$$P_{DRV,ON} = \frac{1}{2} \times \frac{R_{HI} \times V_{DRV} \times Q_G \times f_{DRV}}{R_{HI} + R_{GATE} + R_{G,I}}$$

$$P_{DRV,OFF} = \frac{1}{2} \times \frac{R_{LO} \times V_{DRV} \times Q_G \times f_{DRV}}{R_{LO} + R_{GATE} + R_{G,I}}$$

$$P_{DRV} = P_{DRV,ON} + P_{DRV,OFF} \tag{10}$$

In the above equations, the gate drive circuit is represented by a resistive output impedance and this assumption is valid for MOS-based gate drivers. When bipolar transistors are utilized in the gate drive circuit, the output impedance becomes non-linear and the equations do not yield the correct answers. It is safe to assume that with low value gate resistors (< 5 Ω) most gate drive losses are dissipated in the driver. If R_{GATE} is sufficiently large to limit IG below the output current capability of the bipolar driver, the majority of the gate drive power loss is then dissipated in R_{GATE}.

In addition to the gate drive power loss, the transistors accrue switching losses in the traditional sense due to high current and high voltage being present in the device simultaneously for a short period. In order to ensure the least amount of switching losses, the duration of this time interval must be minimized. Looking at the turn-on and turn-off procedures of the MOSFET, this condition is limited to intervals 2 and 3 of the switching transitions in both turn-on and turn-off operation. These time intervals correspond to the linear operation of the device when the gate voltage is between V_{TH} and $V_{GS,Miller}$, causing changes in the current of the device and to the Miller plateau region when the drain voltage goes through its switching transition.

This is a very important realization to properly design high speed gate drive circuits. It highlights the fact that the most important characteristic of the gate driver is its source-sink current capability around the Miller plateau voltage level. Peak current capability, which is measured at full V_{DRV} across the driver's output impedance, has very little relevance to the actual switching performance of the MOSFET. What really determines the switching times of the device is the gate drive current capability when the gate-tosource voltage, that is, the output of the driver is at approximately 5 V (approximately 2.5 V for logic level MOSFETs).

A crude estimate of the MOSFET switching losses can be calculated using simplified linear approximations of the gate drive current, drain current and drain voltage waveforms during periods 2 and 3 of the switching transitions. First the gate drive currents must be determined for the second and third time intervals, respectively:

$$I_{G2} = \frac{V_{DRV} - 0.5 \times (V_{GS,Miller} + V_{TH})}{R_{HI} + R_{GATE} + R_{G,I}}$$

$$I_{G3} = \frac{V_{DRV} - V_{GS,Miller}}{R_{HI} + R_{GATE} + R_{G,I}} \tag{11}$$

Assuming that IG2 charges the input capacitor of the device from V_{TH} to $V_{GS,Miller}$ and IG3 is the discharge current of the C_{RSS} capacitor while the drain voltage changes from $V_{DS,off}$ to 0 V, the approximate switching times are given as:drain voltage changes from $V_{DS,off}$ to 0 V. The approximate switching times are shown in Equation 12.

$$t2 = C_{ISS} \times \frac{V_{GS,Miller} - V_{TH}}{I_{G2}}$$

$$t3 = C_{RSS} \times \frac{V_{DS,off}}{I_{G3}} \tag{12}$$

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During t2 the drain voltage is $V_{DS,off}$ and the current is ramping from 0A to the load current, IL while in t3 time interval the drain voltage is falling from $V_{DS,off}$ to near 0 V. Again, using linear approximations of the waveforms, the power loss components for the respective time intervals can be estimated as shown in Equation 13.

$$P2 = \frac{t2}{T} \times V_{DS,off} \times \frac{I_L}{2}$$

$$P3 = \frac{t3}{T} \times \frac{V_{DS,off}}{2} \times I_L$$

where

- T is the switching period (13)

The total switching loss is the sum of the two loss components, which yields the following simplified expression shown in Equation 14:

$$P_{SW} = \frac{V_{DS(off)} \times I_L}{2} \times \frac{t2 + t3}{T} \quad (14)$$

Even though the switching transitions are well understood, calculating the exact switching losses is almost impossible. The reason is the effect of the parasitic inductive components significantly alter the current and voltage waveforms, as well as the switching times during the switching procedures. Taking into account the effect of the different source and drain inductances of a real circuit would result in second order differential equations to describe the actual waveforms of the circuit. Since the variables, including gate threshold voltage, MOSFET capacitor values, driver output impedances, and so forth. have a very wide tolerance, the above described linear approximation seems to be a reasonable enough compromise to estimate switching losses in the MOSFET.

2.8 Effects of Parasitic Components

The most profound effect on switching performance is exhibited by the source inductance. There are two sources for parasitic source inductance in a typical circuit, the source bond wire neatly integrated into the MOSFET package and the printed circuit board wiring inductance between the source lead and the common ground. This is usually referenced as the negative electrode of the high frequency filter capacitor around the power stage and the bypass capacitor of the gate driver. Current sense resistors in series with the source can add additional inductance to the previous two components.

There are two mechanisms in the switching procedure that involve the source inductor. At the beginning of the switching transitions the gate current is increasing very rapidly as illustrated in Figure 4 and Figure 5. This current must flow through the source inductance and will be slowed down based on the inductor value. Consequently, the time required to charge/discharge the input capacitance of the MOSFET gets longer, mainly influencing the turn-on and turn-off delays (step 1). Furthermore, the source inductor and the C_{ISS} capacitor form a resonant circuit as shown in Figure 7.

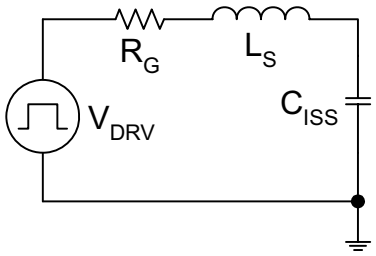

Figure 7. Gate-Drive Resonant Circuit Components

The resonant circuit is exited by the steep edges of the gate drive voltage waveform and it is the fundamental reason for the oscillatory spikes observed in most gate drive circuits. Fortunately, the otherwise very high Q resonance between C_{ISS} and L_S is damped or can be damped by the series resistive components of the loop, which include the driver output impedance, the external gate resistor, and the internal gate mesh resistor.

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The only user adjustable value, R_{GATE}, can be calculated for optimum performance shown in Equation 15.

$$R_{GATE,OPT} = 2 \times \sqrt{\frac{L_S}{C_{ISS}}} - (R_{DRV} + R_{G,I}) \tag{15}$$

Smaller resistor values will result an overshoot in the gate drive voltage waveform, but also result in faster turn-on speed. Higher resistor values will underdamp the oscillation and extend the switching times without offering any benefit for the gate drive design.

The second effect of the source inductance is a negative feedback whenever the drain current of the device is changing rapidly. This effect is present in the second time interval of the turn-on and in the third time interval of the turn-off procedure. During these periods the gate voltage is between V_{TH} and $V_{GS,Miller}$, and the gate current is defined by the voltage across the drive impedance, $V_{DRV} – V_{GS}$. In order to increase the drain current quickly, significant voltage has to be applied across the source inductance. This voltage reduces the available voltage across the drive impedance, which reduces the rate of change in the gate drive voltage and results in a lower di/dt of the drain current. The lower di/dt requires less voltage across the source inductance. A delicate balance of gate current and drain di/dt is established through the negative feedback by the source inductor.

The other parasitic inductance of the switching network is the drain inductance, which is again composed of several components. They are the packaging inductance inside the transistor package, all the inductances associated with interconnection and the leakage inductance of a transformer in isolated power supplies. Their effect can be lumped together since they are in series with each other. They act as a turn-on snubber for the MOSFET. During turn-on they limit the di/dt of the drain current and reduce the drain-to-source voltage across the device by the factor of LD·di/dt. In fact, L_D can reduce the turnon switching losses significantly. While higher LD values seem beneficial at turn-on, they cause considerable problems at turn-off when the drain current must ramp down quickly. To support the rapid reduction in drain current due to the turnoff of the MOSFET, a voltage in the opposite direction with respect to turn-on must be across L_D. This voltage is above the theoretical $V_{DS,off}$ level, producing an overshoot in the drain-tosource voltage and an increase in turn-off switching losses.

Accurate mathematical analysis of the complete switching transitions including the effects of parasitic inductances are available in the literature but points beyond the scope of this document.

3 Ground-Referenced Gate Drive

3.1 PWM Direct Drive

In power supply applications, the simplest way of driving the gate of the main switching transistor is to utilize the gate drive output of the PWM controller as shown in Figure 8.

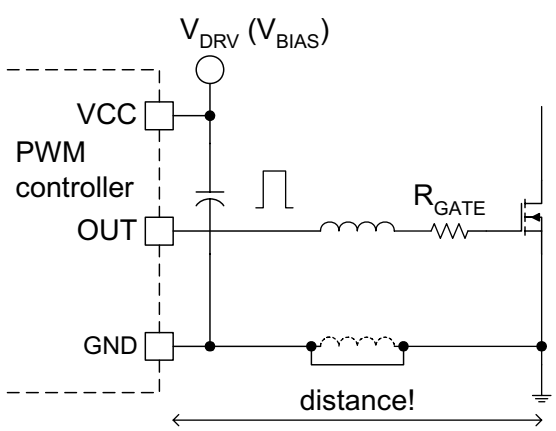

Figure 8. Direct Gate-Drive Circuit

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The most difficult task in direct gate drives is to optimize the circuit layout. As indicated in Figure 8, there might be considerable distance between the PWM controller and the MOSFET. This distance introduces a parasitic inductance due to the loop formed by the gate drive and ground return traces, which can slow down the switching speed and can cause ringing in the gate drive waveform. Even with a ground plane, the inductance can not be completely eliminated since the ground plane provides a low inductance path for the ground return current only. To reduce the inductance linked to the gate drive connection, a wider PCB trace is desirable. Another problem in direct gate drive is the limited drive current capability of the PWM controllers. Very few integrated circuits offer more than 1-A peak gate drive capability. This will limit the maximum die size that can be driven at a reasonable speed by the controller.

Another limiting factor for MOSFET die size with direct gate drive is the power dissipation of the driver within the controller. An external gate resistor can mitigate this problem as discussed before. When direct gate drive is absolutely necessary for space or cost savings, special considerations are required to provide appropriate bypassing for the controller. The high current spikes driving the gate of the MOSFET can disrupt the sensitive analog circuitry inside the PWM controller. As MOSFET die size increases, so too does gate charge required. The selection of the proper bypass capacitor calls for a little bit more scientific approach than picking the usual 0.1 µF or 1 µF bypass capacitor.

3.1.1 Sizing the Bypass Capacitor

In this section, the calculation of the MOSFET gate driver's bypass capacitor is demonstrated. This capacitor is the same as the PWM controller's bypass capacitor in direct gate drive application because that is the capacitor that provides the gate drive current at turn-on. In case of a separate driver circuit, whether a gate drive IC or discrete solution, this capacitor must be placed close, preferably directly across the bias and ground connection of the driver.

There are two current components to consider. One is the quiescent current that can change by a 10x factor based on the input state of some integrated drivers. This itself causes a duty cycle dependent ripple across the bypass capacitor that can be calculated as shown in Equation 16.

$$\Delta V_Q = \frac{I_{Q,HI} \times D_{MAX}}{C_{DRV} \times f_{DRV}}$$

where

- it is assumed that the driver's quiescent current is higher when its input is driven high. (16)

The other ripple component is the gate current. Although the actual current amplitude is not know in most cases, the voltage ripple across the bypass capacitor can be determined based on the value of the gate charge. At turn-on, this charge is taken out of the bypass capacitor and transferred to the MOSFET input capacitor. Accordingly the ripple is shown in Equation 17.

$$\Delta V_{QG} = \frac{Q_G}{C_{DRV}} \tag{17}$$

Using the principle of superposition and solving the equations for CDRV, the bypass capacitor value for a tolerable ripple voltage (ΔV) can be found by using Equation 18.

$$C_{DRV} = \frac{I_{Q,HI} \times \frac{D_{MAX}}{f_{DRV}} + Q_G}{\Delta V}$$

where

- $I_{Q,HI}$ is the quiescent current of the driver when its input is driven high
- D_{MAX} is the maximum duty cycle of the driver while the input can stay high
- f_{DRV} is the operating frequency of the driver
- Q_G is the total gate charge based on the amplitude of the gate drive and drain-tosource off state voltages. (18)

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3.1.2 Driver Protection

Another must-do with direct drive and with gate drive ICs using bipolar output stage is to provide suitable protection for the output bipolar transistors against reverse currents. As indicated in Figure 9, the output stage of the integrated bipolar drivers is built from npn transistors due to their more efficient area utilization and better performance.

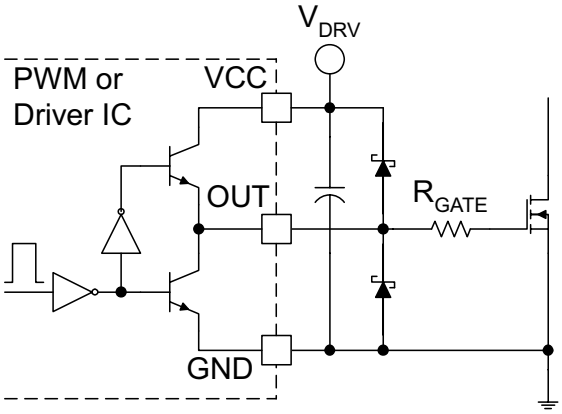

Figure 9. Gate-Drive With Integrated Bipolar Transistors

The npn transistors can handle currents in one direction only. The high side npn can source but can not sink current while the low side is exactly the opposite. Unavoidable oscillations between the source inductor and the input capacitor of the MOSFET during turn-on and turn-off necessitate that current should be able to flow in both directions at the output of the driver. To provide a path for reverse currents, low forward voltage drop Schottky diodes are generally needed to protect the outputs. The diodes must be placed very close to the output pin and to the bypass capacitor of the driver. It is important to point out also, that the diodes protect the driver only, they are not clamping the gate-to-source voltage against excessive ringing especially with direct drive where the control IC might be far away from the gate-source terminals of the MOSFET.

3.2 Bipolar Totem-Pole Driver

One of the most popular and cost effective drive circuit for driving MOSFETs is a bipolar, noninverting totem-pole driver as shown in Figure 10.

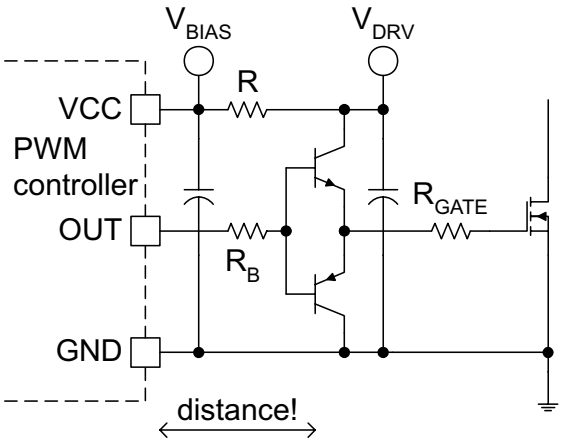

Figure 10. Bipolar Totem-Pole MOSFET Driver

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Like all external drivers, this circuit handles the current spikes and power losses making the operating conditions for the PWM controller more favorable. Of course, they can be and should be placed right next to the power MOSFET they are driving. That way the high current transients of driving the gate are localized in a very small loop area, reducing the value of parasitic inductances. Even though the driver is built from discrete components, it needs its own bypass capacitor placed across the collectors of the upper npn and the lower pnp transistors. Ideally there is a smoothing resistor or inductor between the bypass capacitor of the driver and the bypass capacitor of the PWM controller for increased noise immunity. The R_{GATE} resistor of Figure 10 is optional and RB can be sized to provide the required gate impedance based on the large signal beta of the driver transistors.

An interesting property of the bipolar totem-pole driver that the two base-emitter junctions protect each other against reverse breakdown. Furthermore, assuming that the loop area is really small and R_{GATE} is negligible, they can clamp the gate voltage between VBIAS+VBE and GND-VBE using the base-emitter diodes of the transistors. Another benefit of this solution, based on the same clamp mechanism, is that the npn-pnp totem-pole driver does not require any Schottky diode for reverse current protection.

3.3 MOSFET Totem-Pole Driver

The MOSFET equivalent of the bipolar totempole driver is pictured in Figure 11. All the benefits mentioned about the bipolar totem-pole driver are equally applicable to this implementation.

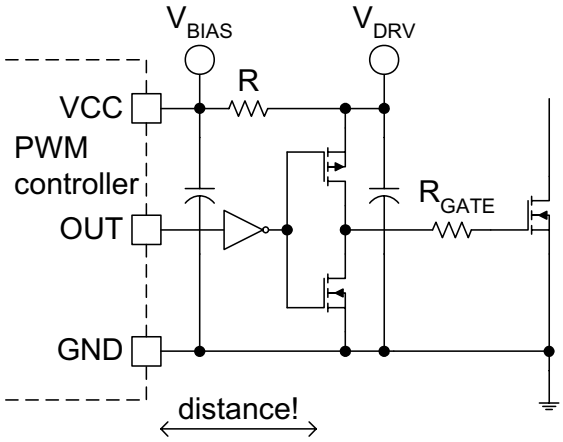

Figure 11. MOSFET-Based Totem-Pole Driver

Unfortunately, this circuit has several drawbacks compared to the bipolar version that explain that it is very rarely implemented discretely. The circuit of Figure 11 is an inverting driver, therefore, the PWM output signal must be inverted. In addition, the suitable MOSFET transistors are more expensive than the bipolar ones and they will have a large shoot through current when their common gate voltage is in transition. This problem can be circumvented by additional logic or timing components, which is extensively used in IC implementations.

3.4 Speed-Enhancement Circuits

When speed enhancement circuits are mentioned, designers exclusively consider circuits that speed-up the turn-off process of the MOSFET. The reason is that the turn-on speed is usually limited by the turn-off, or reverse recovery speed of the rectifier component in the power supply. As discussed with respect to the inductive clamped model in Figure 3, the turn-on of the MOSFET coincides with the turn-off of the rectifier diode. Therefore, the fastest switching action is determined by the reverse recovery characteristic of the diode, not by the strength of the gate drive circuit. In an optimum design the gate drive speed at turn-on is matched to the diode switching characteristic. Considering also that the Miller region is closer to GND than to the final gate drive voltage VDRV, a higher voltage can be applied across the driver output impedance and the gate resistor. Usually the obtained turn-on speed is sufficient to drive the MOSFET.

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The situation is vastly different at turn-off. In theory, the turn-off speed of the MOSFET depends only on the gate drive circuit. A higher current turn-off circuit can discharge the input capacitors quicker, providing shorter switching times and consequently lower switching losses. The higher discharge current can be achieved by a lower output impedance MOSFET driver and/or a negative turn-off voltage in case of the common N-channel device. While faster switching can potentially lower the switching losses, the turn-off speed-up circuits increase the ringing in the waveforms due to the higher turnoff di/dt and dv/dt of the MOSFET. This is something to consider in selecting the proper voltage rating and EMI containment for the power device.

3.4.1 Turn-Off Diode

The following examples of turn-off circuits are demonstrated on simple ground referenced gate drive circuits, but are equally applicable to other implementations discussed later in the document. The simplest technique is the anti-parallel diode, as shown in Figure 12.

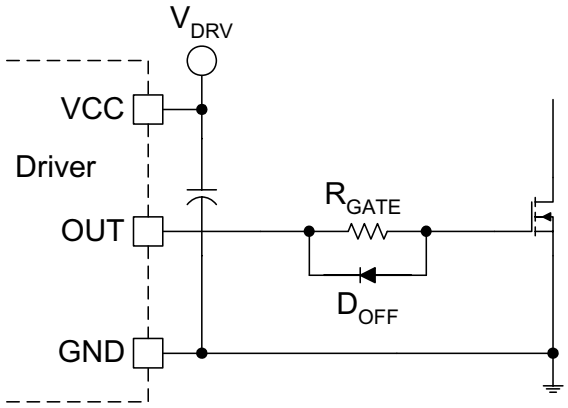

Figure 12. Simple Turn-Off Speed Enhancement Circuit

In this circuit, R_{GATE} allows adjustment of the MOSFET turn-on speed. During turn-off, the antiparallel diode shunts out the resistor. D_{OFF} works only when the gate current is higher than shown in Equation 19.

$$I_G > \frac{V_{D,FWD}}{R_{GATE}} \tag{19}$$

typically around 150 mA, using a 1N4148 and around 300 mA with a BAS40 Schottky antiparallel diode. Consequently, as the gate-to-source voltage approaches 0 V, the diode helps less and less. As a result, this circuit provides a significant reduction in turn-off delay time, but only incremental improvement on switching times and dv/dt immunity. Another disadvantage is that the gate turn-off current still must flow through the driver's output impedance.

3.4.2 PNP Turn-Off Circuit

Undoubtedly the most popular arrangement for fast turn-off is the local pnp turn-off circuit shown in Figure 13. With the help of QOFF, the gate and the source are shorted locally at the MOSFET terminals during turn-off. R_{GATE} limits the turnon speed, and DON provides the path for the turnon current. Also, DON protects the base-emitter junction of QOFF against reverse breakdown at the beginning of the turn-on procedure.

The most important advantage of this solution is that the high peak discharge current of the MOSFET input capacitance is confined in the smallest possible loop between the gate, source and collector, emitter connections of the two transistors.

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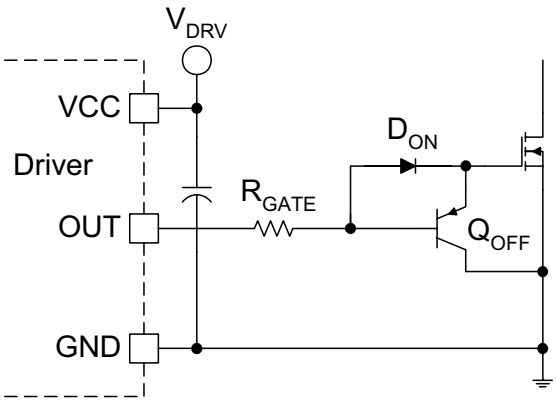

Figure 13. Local pnp Turn-Off Circuit

The turn-off current does not go back to the driver, it does not cause ground bounce problems and the power dissipation of the driver is reduced by a factor of two. The turn-off transistor shunts out the gate drive loop inductance, the potential current sense resistor, and the output impedance of the driver. Furthermore, QOFF never saturates, which is important to be able to turn it on and off quickly. Taking a closer look at the circuit reveals that this solution is a simplified bipolar totem-pole driver, where the npn pull-up transistor is replaced by a diode. Similarly to the totem-pole driver, the MOSFET gate is clamped by the turn-off circuit between GND-0.7V and V_{DRV}+0.7V approximately, eliminating the risk of excessive voltage stress at the gate. The only known shortcoming of the circuit is that it can not pull the gate all the way to 0V because of the voltage drop across the base-emitter junction of QOFF.

3.4.3 NPN Turn-Off Circuit

The next circuit to examine is the local npn turnoff circuit, illustrated in Figure 14. Similarly to the pnp solution, the gate discharge current is well localized. The npn transistor holds the gate closer to GND than its pnp counterpart. Also, this implementation provides a self biasing mechanism to keep the MOSFET off during power up.

Unfortunately, this circuit has some significant drawbacks. The npn turn-off transistor, Q_{OFF} is an inverting stage, it requires an inverted PWM signal provided by Q_{INV}.

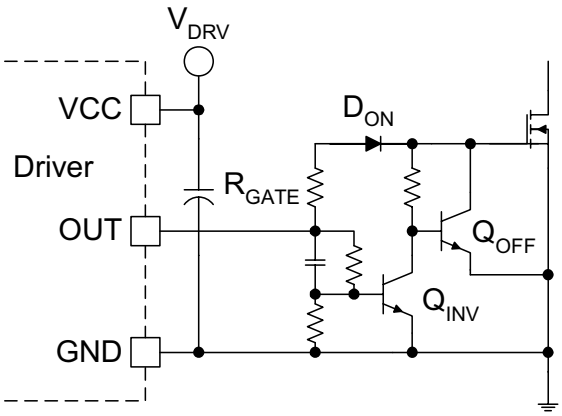

Figure 14. Local NPN Self-Biasing Turn-Off Circuit

The inverter draws current from the driver during the on time of the MOSFET, lowering the efficiency of the circuit. Furthermore, Q_{INV} saturates during the on-time, which can prolong turn-off delay in the gate drive.

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3.4.4 NMOS turn-off circuit

An improved, lower parts count implementation of this principle is offered in Figure 15, using a dual driver to provide the inverted PWM signal for a small N-channel discharge transistor.

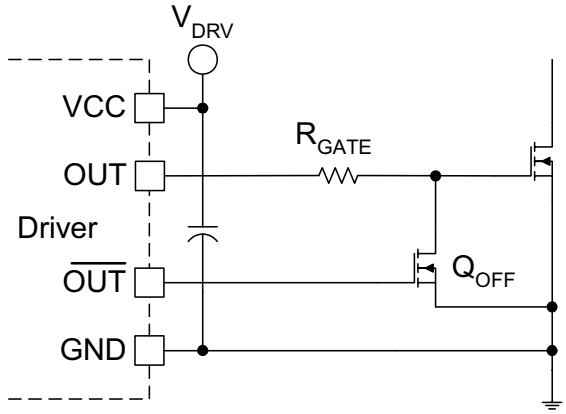

Figure 15. Improved N-Channel MOSFET-Based Turn-off Circuit

This circuit offers very fast switching and complete discharge of the MOSFET gate to 0V. R_{GATE} sets the turn-on speed like before, but is also utilized to prevent any shoot through currents between the two outputs of the driver in case of imperfect timing of the drive signals. Another important fact to consider is that the C_{OSS} capacitance of QOFF is connected in parallel to the C_{ISS} capacitance of the main power MOSFET. This increases the effective "Total Gate Charge" the driver has to provide. Also to consider, the gate of the main MOSFET is floating before the outputs of the driver IC becomes intelligent during power up.

3.5 dv/dt Protection

There are two situations when the MOSFET has to be protected against dv/dt triggered turn-on. One is during power up where protection can usually be provided by a resistor between the gate and source terminals of the device. The pull down resistor value depends on the worst case dv/dt of the power rail during power up according to Equation 20.

$$R_{GS} < \frac{V_{TH}}{C_{GD}} \times \left(\frac{dt}{dv}\right)_{TURN-ON} \tag{20}$$

In this calculation, the biggest challenge is to find the highest dv/dt that can occur during power up and provide sufficient protection for that particular dv/dt.

The second situation is in normal operation when turn-off dv/dt is forced across the drain-to-source terminals of the power switch while it is off. This situation is more common than one may originally anticipate. All synchronous rectifier switches are operated in this mode as will be discussed later. Most resonant and soft switching converters can force a dv/dt across the main switch right after its turn-off instance, driven by the resonant components of the power stage. Since these dv/dt's are significantly higher than during power up and V_{TH} is usually lower due to the higher operating junction temperature, protection must be provided by the low output impedance of the gate drive circuit.

The first task is to determine the maximum dv/dt that can occur under worst case conditions. The next step in evaluating the suitability of a particular device to the application is to calculate its natural dv/dt limit, imposed by the internal gate resistance and the C_{GD} capacitance of the MOSFET. Assuming ideal (zero Ω) external drive impedance the natural dv/dt limit is shown in Equation 21.

$$\frac{dv}{dt}_{LIMIT} = \frac{V_{TH} - 0.007 \times (T_J - 25)}{R_{G,I} \times C_{GD}}$$

where

- V_{TH} is the gate threshold at 25°C
- –0.007 is the temperature coefficient of V_{TH}
- $R_{G,I}$ is the internal gate mesh resistance and C_{GD} is the gate-to-drain capacitor. (21)

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If the natural dv/dt limit of the MOSFET is lower than the maximum dv/dt of the resonant circuit, either a different MOSFET or a negative gate bias voltage must be considered. If the result is favorable for the device, the maximum gate drive impedance can be calculated by rearranging and solving the previous equation according to Equation 22.

$$R_{MAX} = \frac{V_{TH} - 0.007 \times (T_J - 25)}{C_{GD}} \times \left(\frac{dt}{dv}\right)_{MAX}$$

where

- $R_{MAX} = R_{LO} + R_{GATE} + R_{G,I}$. (22)

Once the maximum pull down resistor value is given, the gate drive design can be executed. It should be taken into account that the driver's pull down impedance is also temperature dependent. At elevated junction temperature the MOSFET based gate drive ICs exhibit higher output resistance than at 25°C where they are usually characterized.

Turn-off speed enhancement circuits can also be used to meet dv/dt immunity for the MOSFET since they can shunt out R_{GATE} at turn-off and during the off state of the device. For instance, the simple pnp turn-off circuit of Figure 13 can boost the maximum dv/dt of the MOSFET. The equation modified by the effect of the beta of the pnp transistor yields the increased dv/dt rating shown in Equation 23.

$$\frac{dv}{dt} = \frac{V_{TH} - 0.007 \times (T_J - 25)}{\left(R_{G,J} + \frac{R_{GATE} + R_{LO}}{\beta}\right) \times C_{GD}} \quad (23)$$

In the dv/dt calculations a returning factor is the internal gate resistance of the MOSFET, which is not defined in any data sheet. As pointed out earlier, this resistance depends on the material properties used to distribute the gate signal, the cell density, and the cell design within the semiconductor.

4 Synchronous Rectifier Drive

The MOSFET synchronous rectifier is a special case of ground referenced switches. These devices are the same N-channel MOSFETs used in traditional applications, but applied in low voltage outputs of the power supplies instead of rectifier diodes. They usually work with a very limited drain-to-source voltage swing, therefore, their C_{DS} and C_{GD} capacitors exhibit relatively large capacitance values. Moreover, their application is unique because these devices are operated in the fourth quadrant of their V-I plane. The current is flowing from the source toward the drain terminal. That makes the gate drive signal kind of irrelevant. If the circumstances, other components around the synchronous switch require, current will flow in the device, either through the resistive channel or through the parasitic body diode of the MOSFET. The easiest model to examine the switching behavior of the MOSFET synchronous rectifier is a simplified buck power stage where the rectifier diode is replaced by the QSR transistor as shown in Figure 16.

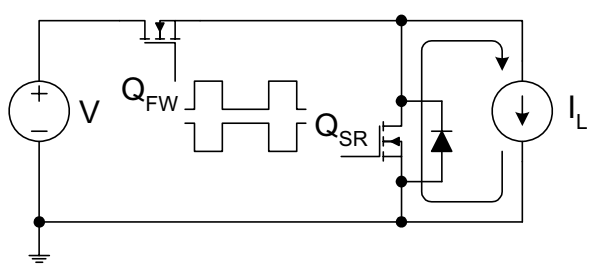

Figure 16. Simplified Synchronous Rectification Model

The first thing to recognize in this circuit is that the operation of the synchronous rectifier MOSFET depends on the operation of another controlled switch in the circuit, namely the forward switch, Q_{FW}. The two gate drive waveforms are not independent and specific timing criteria must be met. Overlapping gate drive signals would be fatal because the two MOSFETs would short circuit the voltage source without any significant current limiting component in the loop. Ideally, the two switches would turn-on and off simultaneously to prevent the body diode of the Q_{SR} MOSFET to turn-on. Unfortunately, the window of opportunity to avoid body diode conduction is very narrow. Very accurate, adaptive timing and fast switching speeds are required, which are usually out of reach with traditional design techniques.

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Consequently, in most cases a brief period – from 20 ns to 80 ns – of body diode conduction precedes the turn-on and follows the turn-off of the synchronous MOSFET switch.

4.1 Gate Charge

During the body diode conduction period, the full load current is established in the device and the drain-to-source voltage equals the body diode forward voltage drop. Under these conditions the required gate charge to turn the device on or off is different from the gate charge needed in traditional first quadrant operation. When the gate is turned-on, the drain-to-source voltage is practically zero and the C_{GD} and C_{DS} capacitors are discharged. Also, the Miller effect is not present, there is no feedback between the drain and gate terminals. Therefore, the required gate charge equals the charge needed to raise the voltage across the gate-to-source and gate-todrain capacitors from 0 V to the final V_{DRV} level. For an accurate estimate, the low voltage average value of the C_{GD} capacitor between 0 V and V_{DRV} has to be determined according to Equation 24.

$$C_{GD,SR} = 2 \times C_{RSS,SPEC} \times \sqrt{\frac{V_{DS,SPEC}}{0.5 \times V_{DRV}}} \tag{24}$$

Equation 25 can then be used to estimate the total gate charge of the synchronous MOSFET rectifier.

$$Q_{Q,SR} = (C_{GS} + C_{GD,SR}) \times V_{DRV} \tag{25}$$

This value is appreciably lower than the total gate charge listed in the MOSFET data sheets. The same MOSFET with an identical driver circuit used for synchronous rectification can be turned on or off quicker than if it would be driven in its first quadrant operation. Unfortunately, this advantage can not be realized since the low $R_{DS(on)}$ devices, applicable for synchronous rectification, usually have pretty large input and output capacitances due to their large die size. Another important note from driver power dissipation point of view is that the total gate charge value from the data sheet should be considered. Although the gate charge delivered by the driver during turn-on is less than the typical number listed in the data sheet, that covers a portion of the total charge passing through the driver output impedance. Before turn-on, while the drain-to-source voltage changes across the device, the Miller charge provided by the power stage must flow through the driver of the synchronous MOSFET causing additional power dissipation. This phenomenon can be seen in Figure 17, which is part of the next discussion on dv/dt considerations.

The turn-off procedure of the synchronous MOSFET obeys the same rules as the turn-on procedure, therefore, all the previous considerations with respect to gate charge are applicable.

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4.2 dv/dt considerations

Figure 17 shows the most important circuit and current components during the turn-on and turnoff procedures of Q_{SR}. Actually, it is more accurate to say that the switching actions taking place in Q_{FW} forces Q_{SR} to turn-on or off independently of its own gate drive signal.

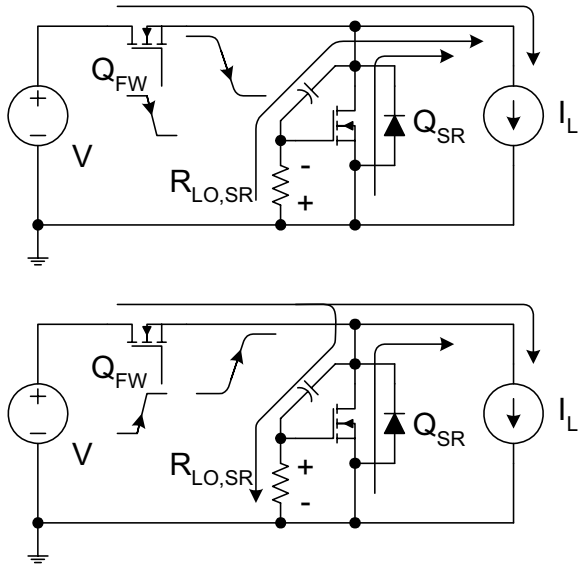

Figure 17. Synchronous Switching Model

The turn-on of Q_{SR} starts with the turn-off of Q_{FW}. When the gate drive signal of Q_{FW} transitions from high to low, the switching node transitions from the input voltage level to GND. The current stays in the forward switch until the C_{RSS} capacitor is discharged and the body diode of Q^{SR} is forward biased. At that instant the synchronous MOSFET takes over the current flow and Q_{FW} turns off completely. After a short delay dominated by the capabilities of the controller, the gate drive signal of Q_{SR} is applied and the MOSFET is turned on. At that time the current transfers from the body diode to the channel of the device.

At the end of the conduction period of Q_{SR}, the MOSFET must be turned off. This procedure is initiated by removing the drive signal from the gate of the synchronous switch. This event itself will not cause the turn-off of the device. Instead, it forces the current to flow in the body diode instead of the channel. The operation of the circuit is indifferent to this change. Current starts to shift from Q_{SR} to Q_{FW} when the gate of the forward switch transitions from low to high. Once the full load current is taken over by Q_{FW} and the body diode is fully recovered, the switching node transitions from GND to the input voltage level. During this transition the C_{RSS} capacitor of Q_{SR} is charged and the synchronous MOSFET is susceptible to dv/dt induced turn-on.

Summarizing this unique operation of the synchronous MOSFET and its gate drive, the most important conclusion is to recognize that both turn-on and turn-off dv/dt of the synchronous MOSFET is forced on the device by the gate drive characteristics (the switching speed) of the forward switch. Therefore, the two gate drive circuits should be designed together to ensure that their respective speed and dv/dt limit matches under all operating conditions. This can be ensured by adhering to the steps of Equation 26.

$$\frac{dv}{dt}_{TURN-ON(FW)} = \frac{V_{DRV} - V_{GS,PLATEAU(FW)}}{(R_{HI(FW)} + R_{GATE(FW)} + R_{G,J(FW)}) \times C_{RSS(FW)}}$$

$$\frac{dv}{dt}_{MAX(SR)} = \frac{V_{TH(SR)}}{(R_{LO(SR)} + R_{GATE(SR)} + R_{G,J(SR)}) \times C_{RSS(SR)}}$$

$$\frac{dv}{dt}_{TURN-ON(FW)} < \frac{dv}{dt}_{MAX(SR)} \tag{26}$$

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Assuming the same devices for Q_{SR} and Q_{FW}, no external gate resistors, and that the internal gate resistance is negligible compared to the drivers output impedance, the ratio of the driver output impedances can be approximated as shown in Equation 27.

$$\frac{R_{LO(SR)}}{R_{HI(FW)}} \leq \frac{V_{TH(SR)}}{V_{DRV} - V_{GS,PLATEAU(FW)}} \tag{27}$$

A typical example with logic level MOSFETs driven by a 10-V drive signal would yield a ratio of 0.417, which means that the pull down drive impedance of Q_{SR} must be less than 42% of the pull up drive impedance of Q_{FW}. When carrying out these calculations, remember that every parameter except V_{DRV} is temperature dependent and their values might have to be adjusted to reflect the worst case operating conditions of the design.

5 High-Side Non-Isolated Gate Drives

High-side non-isolated gate drive circuits can be classified by the device type they are driving or by the type of drive circuit involved. Accordingly, they are differentiated whether P-channel or N-channel devices are used or whether they implement direct drive, level shifted drive, or bootstrap technique. Whichever way, the design of high side drivers need more attention and the following checklist might be useful to cover all aspects of the design:

- Efficiency
- Bias and power requirements
- Speed limitations
- Maximum duty-cycle limit
- dv/dt implications
- Start-up conditions
- Transient operation
- Bypass capacitor size
- Layout, grounding considerations

5.1 High-Side Drivers for P-Channel Devices

In this group of circuits the source terminal of the P-channel MOSFET switch is connected to the positive input rail. The driver applies a negative amplitude turn-on signal to the gate with respect to the source of the device. This means that the output of the PWM controller has to be inverted and referenced to the positive input rail. Because the input voltage can be considered as a DC voltage source, high side P-channel drivers do not have to swing between large potential differences on the switching frequency basis, but they must work over the entire input voltage range. Moreover, the driver is referenced to an AC ground potential due to the low AC impedance of the input voltage source.

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5.1.1 P-Channel Direct Drive

The easiest case of P-channel high side drivers is direct drive, which can be implemented if the maximum input voltage is less then the gate-tosource breakdown voltage of the device. A typical application area is 12 V input DC/DC converters using a P-channel MOSFET, similar to the schematic in Figure 18. Note the inverted PWM output signal is readily available in some dedicated controllers for P-channel devices.

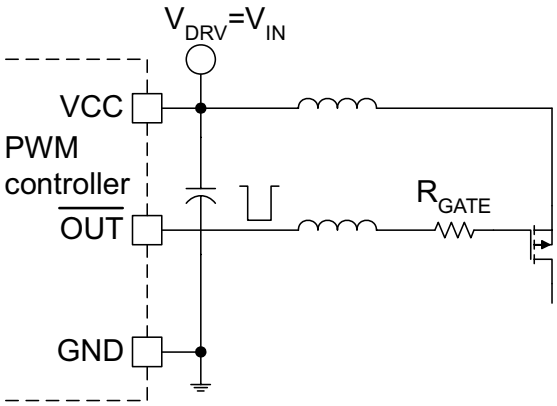

Figure 18. Direct Drive for P-Channel MOSFET

The operation of the circuit is similar to the ground referenced direct driver for N-channel devices. The significant difference is the path of the gate drive current, which never flows in the ground connections. Instead, the high charge and discharge currents of the gate are conducted by the positive rail interconnection. Consequently, to minimize the loop inductance in the gate drive, wide traces or a plane is desirable for the positive input.

5.1.2 P-Channel Level-Shifted Drive

For input voltages exceeding the gate-to-source voltage limit of the MOSFET, level shifted gate drive circuits are necessary. The simplest level shift technique is using an open collector driver as shown in Figure 19. Unfortunately, open collector level shifters are not suitable for driving MOSFETs directly in a high speed application.

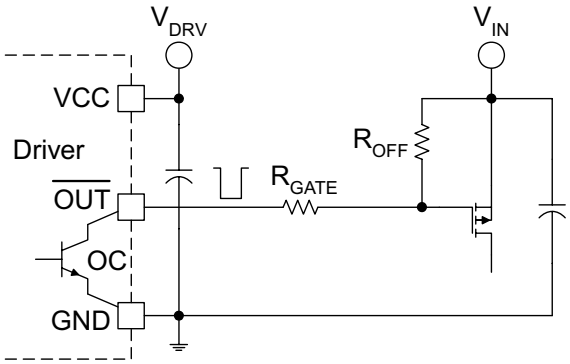

Figure 19. Open Collector Drive for PMOS Device

Problems are numerous with this implementation starting with the limited input voltage range due to the voltage rating of the open collector transistor. But the most inhibiting obstacle is the high drive impedance. Both resistors, R_{OFF} and R_{GATE} must be a high value resistor to limit the continuous current in the driver during the conduction period of the switch. Furthermore, the gate drive amplitude depends on the resistor divider ratio and the input voltage level. Switching speed and dv/dt immunity are severely limited, which excludes this circuit from switching applications. Nevertheless, this very simple level shift interface can be used for driving switches in inrush current limiters or similar applications where speed is not an important consideration.

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Figure 20 shows a level shifted gate drive circuit that is suitable for high speed applications and works seamlessly with regular PWM controllers. The open collector level shift principle can be easily recognized at the input of a bipolar totempole driver stage. The level shifter serves two purposes in this implementation; it inverts the PWM output and references the PWM signal to the input rail.

The turn-on speed is fast, defined by R_{GATE} and R_2. During the on-time of the switch a small DC current flows in the level shifter keeping the driver biased in the right state. Both the gate drive power and the level shift current are provided by the positive input of the power stage, which is usually well bypassed.

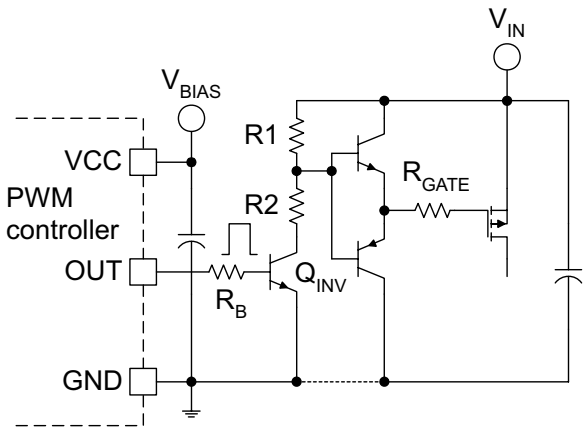

Figure 20. Level-Shifted P-Channel MOSFET Driver

The power consumption of the driver has a frequency dependent portion based on the gate charge of the main switch and a duty-cycle and input voltage dependent portion due to the current flowing in the level shifter.

$$P_{DRIVE} = Q_G \times V_{DRV} \times f_{DRV} + \frac{V_{IN} \times D_{MAX}}{R1 + R2} \tag{28}$$

One of the drawbacks of this circuit is that V_{DRV} is still a function of the input voltage due to the R1, R2 divider. In most cases protection circuits might be needed to prevent excessive voltage across the gate-to-source terminals. Another potential difficulty is the saturation of the npn level shift transistor, which can extend the turnoff time otherwise defined by R1 and R_{GATE}. Fortunately both of these shortcomings can be addressed by moving R2 between the emitter of Q_{INV} and GND. The resulting circuit provides constant gate drive amplitude and fast, symmetrical switching speed during turn-on and turn-off. The dv/dt immunity of the driver scheme is primarily set by the R1 resistor. A lower value resistor will improve the immunity against dv/dt induced turn-on but also increases the power losses of the level shifter. Also, notice that this solution has a built in self-biasing mechanism during power up. While the PWM controller is still inactive, Q_{INV} is off and the gate of the main MOSFET is held below its threshold by R1 and the upper npn transistor of the totempole driver. Pay specific attention to rapid input voltage transients though as they could cause dv/dt induced turn-on during the off state of the P-channel MOSFET transistor.

In general, the DC level shift drivers have relatively low efficiency and are power dissipation limited above a certain input voltage level. The fundamental trade-off is to balance the switching speed and the power consumption of the level shifter to meet all requirements under the entire input voltage range.

5.2 High-Side Direct Drivers for N-Channel Devices

The majority of power supply applications utilize N-channel MOSFETs as the main power switch because of their lower price, higher speed and lower on-resistance. Using N-channel devices as a high side switch necessitates a gate drive circuit that is referenced to the source of the MOSFET. The driver must tolerate the violent voltage swings occurring during the switching transitions and drive the gate of the MOSFET above the positive supply rail of the power supply. In most cases, the gate drive voltage must be above the highest DC potential available in the circuit. All these difficulties make the high side driver design a challenging task.

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5.2.1 High-Side Direct Drive for N-Channel MOSFET

In the easiest high side applications the MOSFET can be driven directly by the PWM controller or by a ground referenced driver. Two conditions must be met for this application:

$$V_{DRV} < V_{GS,MAX}$$

$$V_{IN} < V_{DRV} - V_{GS,Miller} \tag{29}$$

A typical application schematic is illustrated in Figure 21 with an optional pnp turn-off circuit.

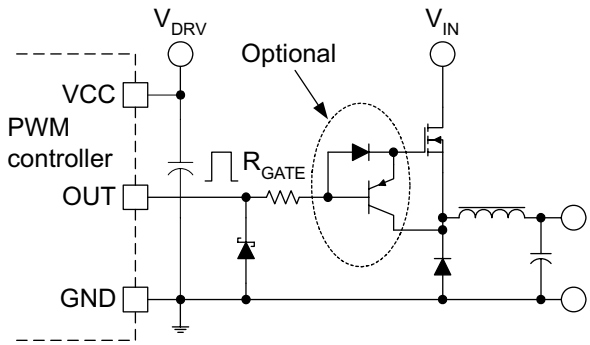

Figure 21. Direct Drive of N-Channel MOSFET

Looking at the basic operation of the circuit – neglect the pnp turn-off transistor for now – there are two major differences with this configuration compared to the ground referenced drive scheme. Since the drain is connected to the positive DC input rail, the switching action takes place at the source terminal of the device. It is still the same clamped inductive switching with identical turnon and turn-off intervals. But from gate drive design point of view this is a completely different circuit. Notice that the gate drive current can not return to ground at the source terminal. Instead it must go through the load, connected to the source of the device. In discontinuous inductor current mode the gate charge current must go through the output inductor and the load. In continuous inductor current mode, however, the loop can be closed through the conducting pn junction of the rectifier diode. At turn-off, the gate discharge current comes through the rectifier diode connected between ground and the source of the MOSFET. In all operating modes, both the charge and discharge currents of the C_{GD} capacitor flow through the high frequency bypass capacitor of the power stage.

The net result of all these differences is the increased parasitic source inductance due to more components and larger loop area involved in the gate drive circuitry. As presented earlier, the source inductance has a negative feedback effect on the gate drive and slows down the switching actions in the circuit.

The other significant difference in high side direct drive is the behavior of the source – the switching node of the circuit. Paying close attention to the source waveform of the MOSFET during turn-off, a large negative voltage can be observed. Figure 22 illustrates this rather complex switching action.

As the turn-off is initiated by pulling the gate terminal toward ground, the input capacitances of the MOSFET are quickly discharged to the Miller plateau voltage. The device is still fully on, the entire load current is flowing through the drain to the source and the voltage drop is small. Next, in the Miller region, the MOSFET works as a source follower.

The source falls together with the gate, and while the voltage across the drain-to-source increases, the gate-to-source voltage remains constant at the $V_{GS,Miller}$ level. The dv/dt is limited by the gate drive impedance and the C_{GD} capacitor of the device. Once the source falls 0.7 V or so below ground, the rectifier diode is supposed to clamp the switching node to ground.

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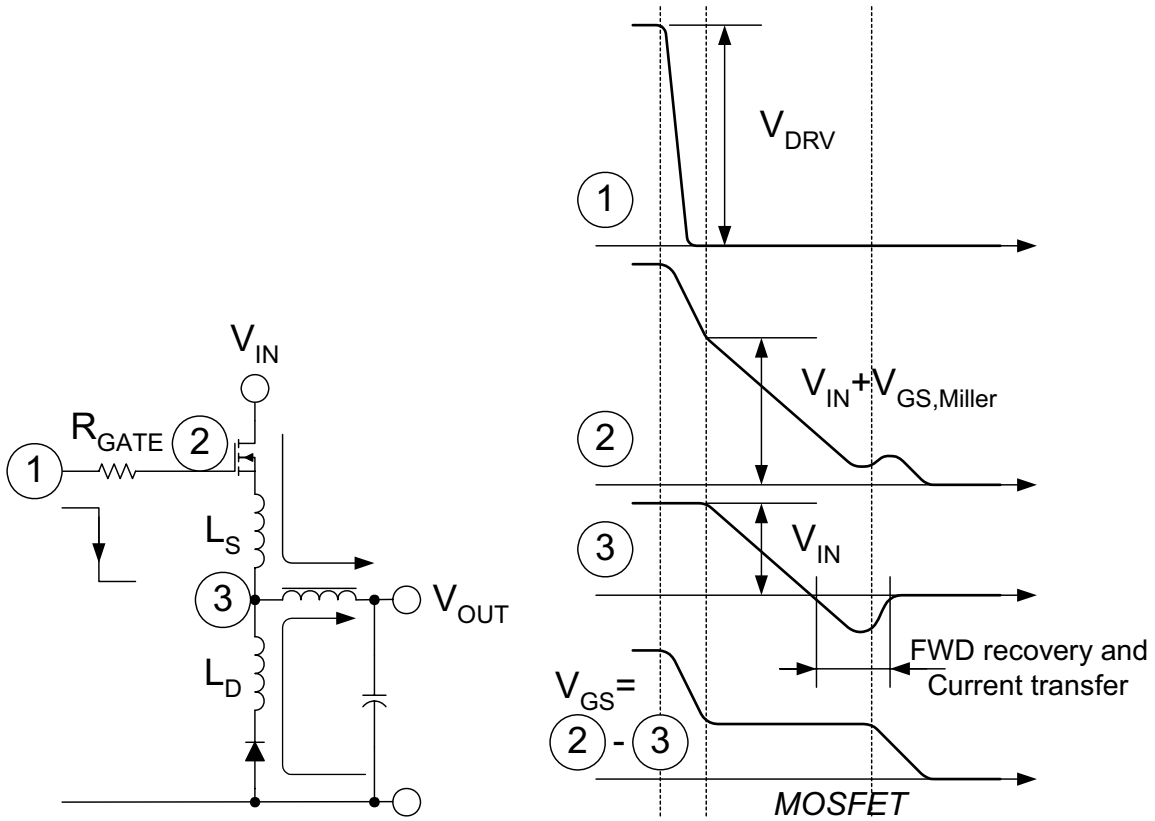

Figure 22. Turn-Off of High-Side N-Channel MOSFET

Actually, the source can fall way below ground for a short period of time until the rectifier diode gets through its forward recovery process and the current overcomes the effect of the parasitic inductances. After the load current is completely transferred from the MOSFET to the diode, the switching node can return to its final voltage, a diode drop below ground.

This negative excursion of the source voltage represents a significant problem for the gate drive circuit. Slow diodes, high parasitic inductance values can cause excessive negative voltage at the source of the MOSFET, and can pull the output pin of the driver below ground. To protect the driver, a low forward voltage drop Schottky diode might be connected between the output pin and ground as indicated in Figure 21. Another aspect to consider is when the gate terminal reaches 0 V, the gate discharge current would become zero. Further negative pull on the gate terminal and the MOSFET starts turning back on. Ultimately the system finds a very delicate equilibrium where the gate discharge current and the voltage drop across the parasitic inductances result the same di/dt in the device current.

Even the optional turn-off speed-up circuit shown in Figure 21 can not help during the negative voltage spike of the switching junction. The pnp transistor will turn-off when the gate falls to a VBE above ground and the MOSFET is left on its own during the negative voltage transient. Also, pay attention to the reduced noise tolerance during the off state of the main switch. The source is several hundred millivolts below ground and the gate is held at approximately 0.7 V above ground. This positive voltage across the gate with respect to the source is dangerously close to the threshold voltage especially for logic level devices and at elevated temperatures.

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5.2.2 Bootstrap Gate-Drive Technique

Where input voltage levels prohibit the use of direct gate drive circuits for high side N-channel MOSFETs, the principle of bootstrap gate drive technique can be considered. This method utilizes a gate drive and accompanying bias circuit, both referenced to the source of the main MOSFET transistor. Both the driver and the bias circuit swing between the two input voltage rails together with the source of the device. However, the driver and its floating bias can be implemented by low voltage circuit elements since the input voltage is never applied across their components. The driver and the ground referenced control signal are linked by a level shift circuit, which must tolerate the high voltage difference and considerable capacitive switching currents between the floating high side and ground referenced low side circuits.

5.2.2.1 Discrete High-Performance Floating Driver

A typical implementation representing the bootstrap principle is displayed in Figure 23 . The ground referenced PWM controller or MOSFET driver is represented by its local bypass capacitor and the output pin. The basic building blocks of the bootstrap gate drive circuit can be easily recognized. The level-shift circuit is comprised of the bootstrap diode Q_{BST}, R1, R2 and the level shift transistor, Q_{LS}. The bootstrap capacitor, C_{BST}, a totem-pole bipolar driver and the usual gate resistor are the floating, source referenced part of the bootstrap solution.

This particular implementation can be used very effectively in 12 V to approximately 24 V systems with simple low cost PWM controllers that have no floating driver on board. It is beneficial that the IC voltage rating does not limit the input voltage level. Furthermore, the level shift circuit is a source switched small NMOS transistor that does not draw any current during the on time of the main MOSFET from the bootstrap capacitor. It is an important feature to maintain high efficiency in the level shifter, and to extend the maximum on-time of the main switch. The operation can be summarized as follows: when the PWM output goes high to turn on the main MOSFET, the level shift transistor turns off. R1 supports the base current to the upper npn transistor in the totem-pole driver and the main MOSFET turns on. The gate charge is taken from the bootstrap capacitor, C_{BST}. As the switch turns on, its source swings to the positive input rail. The bootstrap diode and transistor block the input voltage and power to the driver is provided from the bootstrap capacitor. At turn-off, the PWM output goes low turning on the level shift transistor.

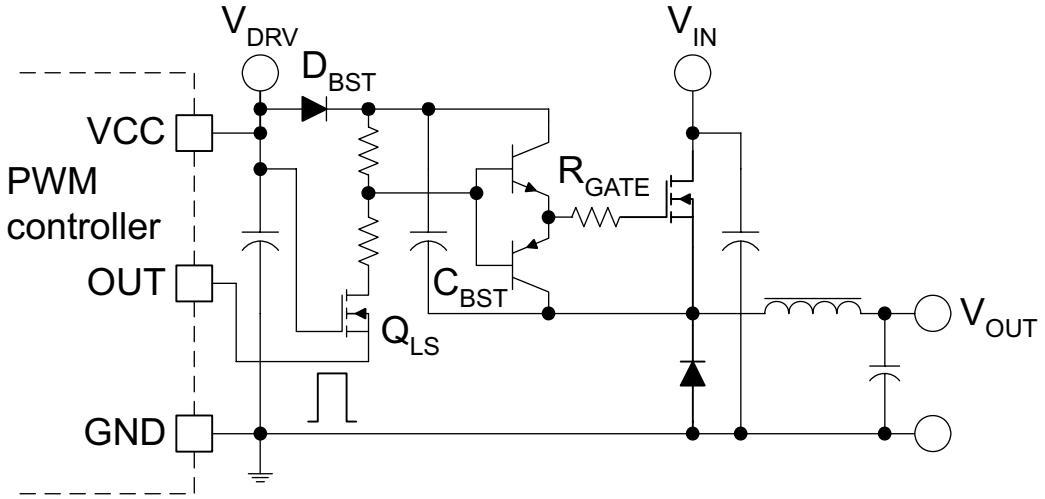

Figure 23. Integrated Bootstrap Driver

Current starts to flow in R1 and R2 towards ground and the lower pnp transistor of the totempole driver turns on. As the gate of the main MOSFET discharges, the drain-to-source voltage increases and the source transitions to ground, allowing the rectifier to turn-on. During the off time of the main switch, the bootstrap capacitor is recharged to the V_{DRV} level through the bootstrap diode. This current is supplied by the C_{DRV} bypass capacitor of the ground referenced circuitry and it goes through D_{BST}, C_{BST}, and the conducting rectifier component. This is the basic operating principle of the bootstrap technique.

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5.2.2.2 Integrated Bootstrap Drivers

In medium input voltage applications, mainly 24 V or 48 V telecom systems, most of the bootstrap components can be integrated into the PWM controller as illustrated in Figure 24.

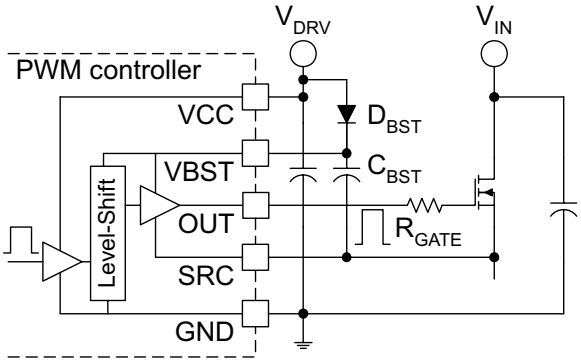

Figure 24. Integrated Bootstrap Driver

For even higher voltages, dedicated driver ICs are available to ease the design of bootstrap gate drive with up to 600-V rating. These high voltage ICs are differentiated by their unique level shift design. In order to maintain high efficiency and manageable power dissipation, the level shifters should not draw any current during the on-time of the main switch. Even a modest 1-mA current in the level shift transistors might result in close to 0.5-W worst-case power dissipation in the driver IC.

A widely used technique for these applications is called pulsed latch level translators and they are revealed in Figure 25.

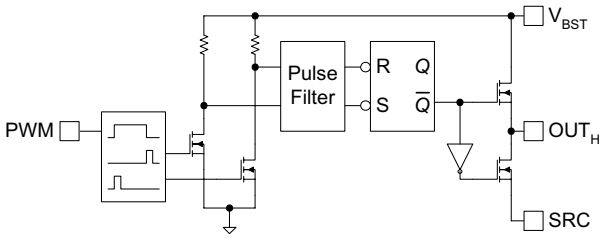

Figure 25. Typical Level-Shifter in High-Voltage Driver IC

As indicated in the drawing, the PWM input signal is translated to ON/OFF commands. The short pulses generated at the rising and falling edges drive the level shift transistor pair that interfaces with the high side circuitry. Accordingly, the floating portion of the driver is modified as well, the level shifted command signals have to be differentiated from noise and must be latched for proper action. This operation results in lower power dissipation because of the short duration of the current in the level shifter but lowers noise immunity since the command signal is not present at the input of the driver continuously. The typical pulse width in a 600 V rated pulsed latch level translator is around 120 nanoseconds. This time interval adds to natural delays in the driver and shows up as turn-on and turn-off delays in the operation and is indicated in the data sheet of the drivers. Due to the longer than optimum delays, the operating frequency range of the high voltage gate driver ICs is limited below a couple of hundreds of kHz. Some lower voltage high side driver ICs (up to 100 V) use continuous current DC level shift circuits to eliminate the delay of the pulse discriminator, therefore, they support higher operating frequency.

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5.2.2.3 Bootstrap Switching Action

Bootstrap gate drive circuits are used with high side N-channel MOSFET transistors as shown in Figure 26. The switching transitions of the high side switch were explored previously with respect to the high side N-channel direct drive scheme and are equally applicable with bootstrap drivers.

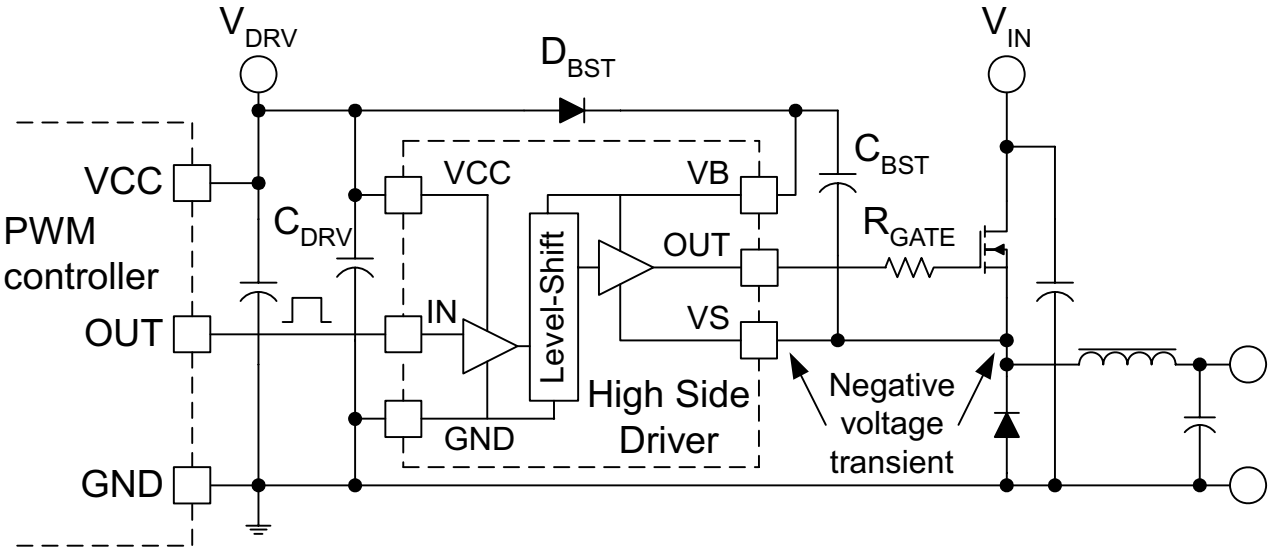

Figure 26. High Voltage Driver IC for Bootstrap Gate Drive

The biggest difficulty with this circuit is the negative voltage present at the source of the device during turn-off. As shown previously, the amplitude of the negative voltage is proportional to the parasitic inductance connecting the source of the main MOSFET to ground (including the parasitic inductance associated with the rectifier) and the turn-off speed (di/dt) of the device as determined primarily by the gate drive resistor, R_{GATE} and input capacitor, C_{ISS}. This negative voltage can be serious trouble for the driver's output stage since it directly affects the source pin – often called SRC or VS pin – of the driver or PWM IC and might pull some of the internal circuitry significantly below ground.

The other problem caused by the negative voltage transient is the possibility to develop an over voltage across the bootstrap capacitor. Capacitor CBST will be peak charged by D_{BST} from C_{DRV}. Since C_{DRV} is referenced to ground, the maximum voltage that can build onto the bootstrap capacitor is the sum of V_{DRV} and the amplitude of the negative voltage at the source terminal. A small resistor in series with the bootstrap diode can mitigate the problem. Unfortunately, the series resistor does not provide a foolproof solution against an over voltage and it also slows down the recharge process of the bootstrap capacitor.

A circuit to deliver very effective protection for the SRC pin is given in Figure 27. It involves relocating the gate resistor from the gate to the source lead between the driver and the main MOSFET and adding a small, low forward voltage drop Schottky diode from ground to the SRC pin of the driver.

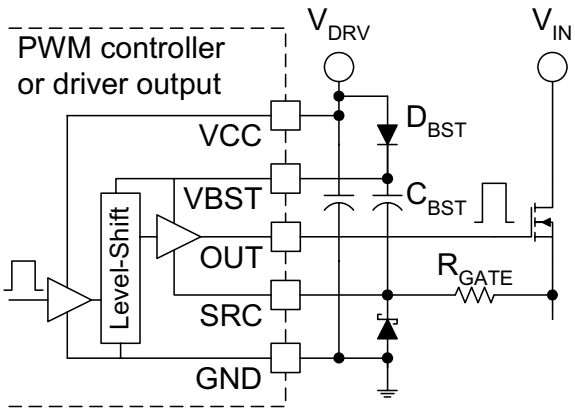

Figure 27. Protecting the SRC Pin

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In this circuit, R_{GATE} has a double purpose; it sets the turn-on and turn-off speed in the MOSFET and also provides current limiting for the Schottky diode during the negative voltage transient of the source terminal of the main switch. Now, the switching node can swing several volts below ground without disturbing the operation of the driver. In addition, the bootstrap capacitor is protected against over voltage by the two diodes connected to the two ends of C_{BST}.

The only potential hazard presented by this circuit is that the charge current of the bootstrap capacitor must go through R_{GATE}. The time constant of CBST and R_{GATE} slows the recharge process, which might be a limiting factor as the PWM duty ratio approaches unity.

5.2.2.4 Bootstrap Biasing, Transient Issues and Start-Up

Figure 28 shows a typical application diagram of the bootstrap gate drive technique. There are four important bypass capacitors marked on the schematic.

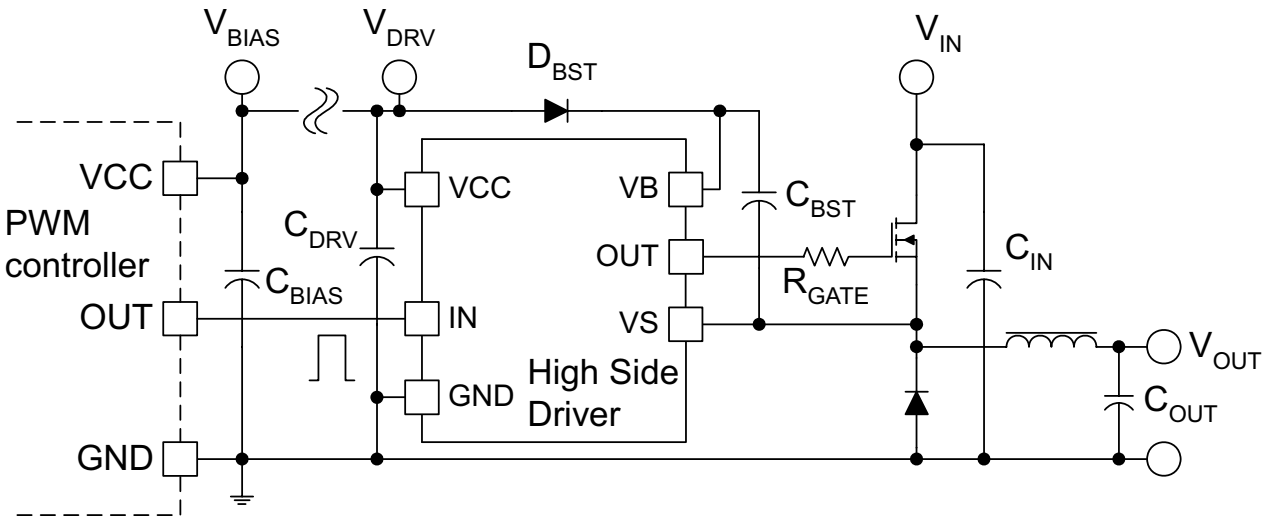

Figure 28. Bootstrap Bypassing Example

The bootstrap capacitor, C_{BST} is the most important component from the design point of view, since it has to filter the high peak current charging the gate of the main MOSFET while providing bias for the source referenced floating circuitry. In every switching cycle during normal operation, the bootstrap capacitor provides the total gate charge (Q_G) to turn-on the MOSFET, the reverse recovery charge (Q_{RR}) and leakage current of the bootstrap diode ($I_{LK,D}$), the quiescent current of the level shifter ($I_{Q,LS}$) and the gate driver ($I_{Q,DRV}$), and the leakage current between the gate-source terminals (I_{GS}), including the current drawn by a potential gate-to-source pull down resistor. Some of these currents flow only during the on-time of the main switch and some of them might be zero depending on the actual implementation of the driver and level shifter.

Assuming steady state operation, use Equation 30 to calculate the bootstrap capacitor value to achieve the targeted ripple voltage, ΔV_{BST}:

$$C_{BST} = \frac{Q_G + Q_{RR} + I_{BST} \times \frac{D_{MAX}}{f_{DRV}}}{\Delta V_{BST}}$$

where

- $I_{BST} = I_{LK,D} + I_{Q,LS} + I_{Q,DRV} + I_{GS}$ (30)

To finalize the bootstrap capacitor value, two extreme operating conditions must be checked as well. During load transients it might be necessary to keep the main switch on or off for several switching cycles. In order to ensure uninterrupted operation under these circumstances, the C_{BST} capacitor must store enough energy to hold the floating bias voltage above the under voltage lockout threshold of the high side driver IC for an extended period of time.

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Going from light load to heavy load, certain controllers can keep the main switch on continuously until the output inductor current reaches the load current value. The maximum on time ($t_{ON,MAX}$) is usually defined by the value and the voltage differential across the output inductor. For these cases, a minimum bootstrap capacitor value can be established as shown in Equation 31.

$$C_{BST,MIN} = \frac{Q_G + Q_{RR} + I_{BST} \times t_{ON,MAX}}{V_{BST} - V_{UVLO}}$$

where

- V_{BST} is the initial value of the bootstrap bias voltage across C_{BST}
- V_{UVLO} is the undervoltage lockout threshold of the driver (31)

With a discrete floating driver implementation, VUVLO could be substituted by the minimum safe gate drive voltage.

Any load transient in the other direction will require pulse skipping when the MOSFET stays off for several switching cycles. When the output inductor current reaches zero, the source of the main switch will settle at the output voltage level. The bootstrap capacitor must supply all the usual discharge current components and store enough energy to be able to turn-on the switch at the end of the idle period. Similar to the previous transient mode, a minimum capacitor value can be calculated as shown in Equation 32.

$$C_{BST,MIN} = \frac{Q_G + (I_{LK,D} + I_{Q,LS} + I_{Q,DRV}) \times t_{OFF,MAX}}{V_{BST} - V_{UVLO}} \quad (32)$$

In certain applications, like in battery chargers, the output voltage might be present before input power is applied to the converter. In these cases, the source of the main MOSFET and the negative node of C_{BST} are sitting at the output voltage and the bootstrap diode might be reverse biased at start-up. Delivering the initial charge to the bootstrap capacitor might not be possible depending on the potential difference between the bias and output voltage levels. Assuming there is enough voltage differential between the input and output voltages, a simple circuit comprised of R_{START} resistor, D_{START} diode, and D_Z zener diode can solve the start-up problem as shown in Figure 29.

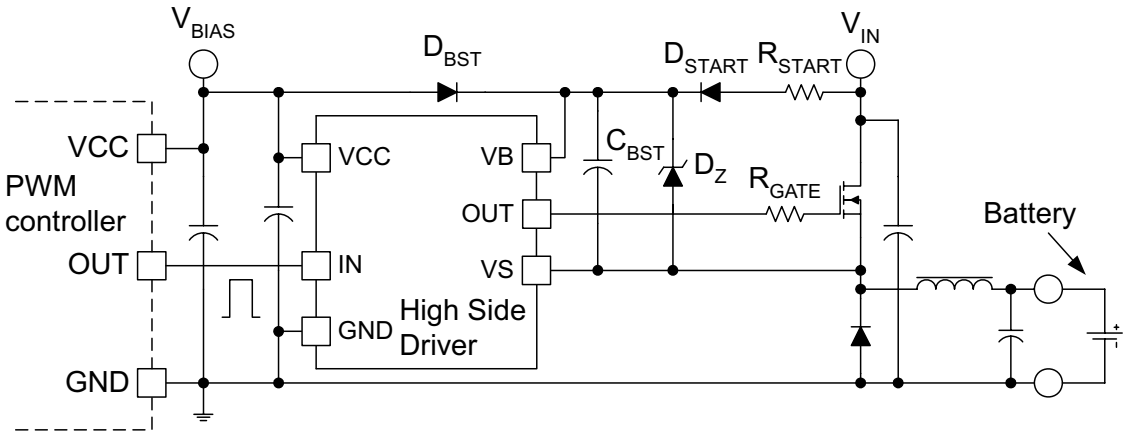

Figure 29. Bootstrap Start-Up Circuit

In this start-up circuit, D_{START} serves as a second bootstrap diode used for charging the bootstrap capacitor at power up. C_{BST} will be charged to the zener voltage of D_Z, which is supposed to be higher than the driver's bias voltage during normal operation. The charge current of the bootstrap capacitor and the zener current are limited by the start-up resistor. For best efficiency, select the value of R_{START} to limit the current to a low value since the second bootstrap path through the start-up diode is permanently in the circuit.

5.2.2.5 Grounding Considerations

There are three important grounding issues that have to be addressed with respect to the optimum layout design of the bootstrap gate drivers with high side N-channel MOSFETs. Figure 28 can be used to identify the most critical high-current loops in a typical application.

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The first focus is to confine the high peak currents of the gate in a minimal physical area. Considering the path the gate current must pass through, it might be a challenging task. At turnon, the path involves the bootstrap capacitor, the turn-on transistor of the driver, the gate resistor, the gate terminal, and finally, the loop is closed at the source of the main MOSFET where C_{BST} is referenced. The turn-off procedure is more complicated as the gate current has two separate components. The discharge current of the C_{GS} capacitor is well localized, it flows through the gate resistor, the turn-off transistor of the driver and from the source to the gate of the power MOSFET. On the other hand, the C_{GD} capacitor's current must go through R_{GATE}, the turn-off transistor of the driver, the output filter, and finally the input capacitor of the power stage (CIN). All three loops carrying the gate drive currents have to be minimized on the printed circuit board.

The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor of the driver, and the rectifier diode or transistor of the power stage. C_{BST} is recharged on the cycle-by-cycle basis through the bootstrap diode from the ground referenced driver capacitor, C_{DRV}, connected from the anode of D_{BST} to ground. The recharge happens in a short time interval and involves high peak current. Therefore, the high side driver must be bypassed locally on its input side as well. According to the rule-of-thumb, C_{DRV} should be an order of magnitude larger than C_{BST}. Minimizing this loop area on the printed circuit board is equally important to ensure reliable operation.

The third issue with the circuit is to contain the parasitic capacitive currents flowing between power ground and the floating circuitry in a low impedance loop. The goal is to steer these currents away from the ground of the sensitive analog control parts. Figure 30 reveals the parasitic capacitive current paths in two representative applications with high side driver ICs.

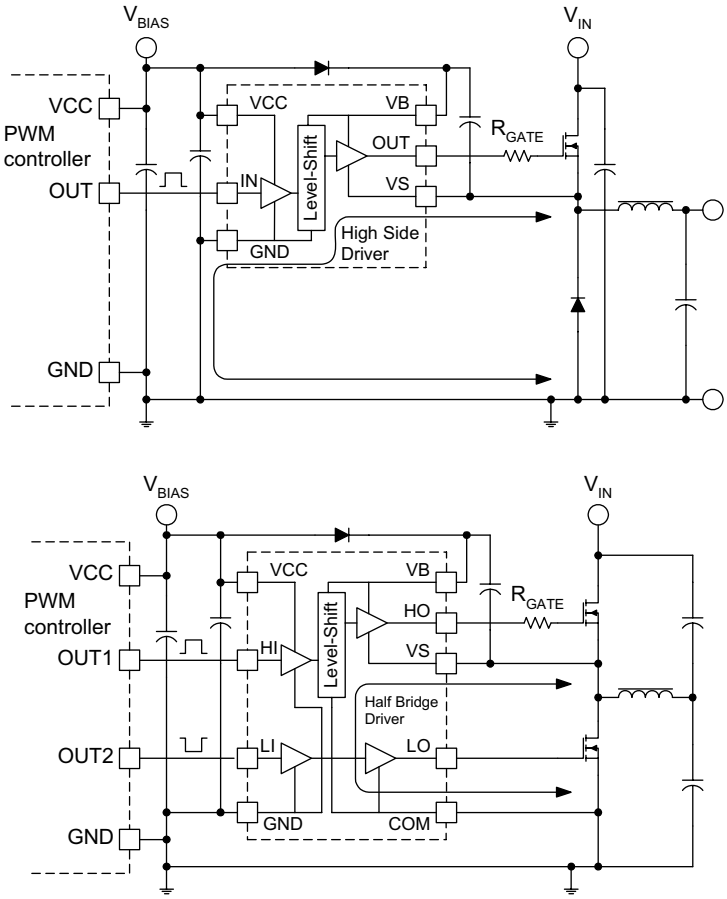

Figure 30. Capacitive Currents in High-Side Applications

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Single high side driver ICs usually have only one GND connection. Since the capacitive currents must return to the ground potential of the power stage, the low side portion of the IC should be referenced to power ground. This is counterintuitive, since the control signal of the driver is referenced to signal ground. Nevertheless, eliminating the high capacitive current component between analog and power ground will also ensure that the potential difference between the two grounds are minimized.

The situation is greatly improved with the general purpose half bridge driver ICs, which contain one low side and one high side driver in the same package. These circuits have two ground connections usually labeled as GND and COM, providing more flexibility in layout. To return the capacitive currents to power ground in the shortest possible route, the COM pin is connected to power ground. The GND pin can be utilized to provide connection to the signal ground of the controller to achieve maximum noise immunity.

For completeness, the bypass capacitor of the PWM controller should be mentioned as well, which is placed near to the V_{CC} and GND pins of the IC. Referring to Figure 28 again, C_{BIAS} is a relatively small capacitor with respect to C_{BST} and C_{DRV} since it provides only high frequency bypassing and it is not involved in the gate drive process.

6 AC-Coupled Gate-Drive Circuits

AC coupling in the gate drive path provides a simple level shift for the gate drive signal. The primary purpose of AC coupling is to modify the turn-on and turn-off gate voltages of the main MOSFET as opposed to high side gate drives where the key interest is to bridge large potential differences. In a ground referenced example like the one in Figure 31, the gate is driven between $-V_{CL}$ and $V_{DRV-VCL}$ levels instead of the original output voltage levels of the driver, 0 V and V_{DRV}. The voltage, V_{CL} is determined by the diode clamp network and it is developed across the coupling capacitor. The benefit of this technique is a simple way to provide negative bias for the gate at turn-off and during the off state of the switch to improve the turn-off speed and the dv/dt immunity of the MOSFET. The trade-off is slightly reduced turn-on speed and potentially higher $R_{DS(on)}$ resistance because of the lower positive drive voltage.

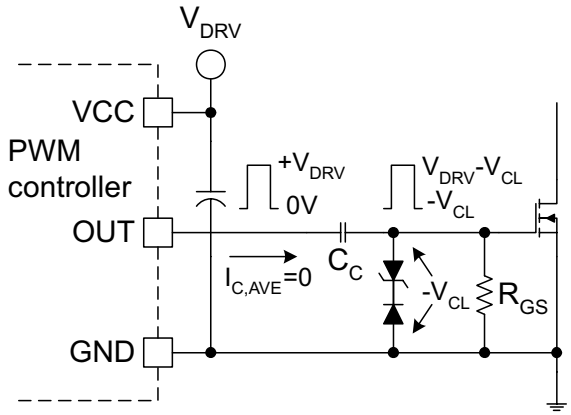

Figure 31. Capacitively-Coupled MOSFET Gate Drive

The fundamental components of AC coupling are the coupling capacitor C_C and the gate-to-source load resistor R_{GS}.

The resistor plays a crucial role during power up, pulling the gate low. This is the only mechanism keeping the MOSFET off at start up due to the blocking effect of the coupling capacitor between the output of the driver and the gate of the device. In addition, R_{GS} provides a path for a current across the coupling capacitor. Without this current component the voltage would not be allowed to build across C_C. Theoretically, in every switching cycle the same amount of total gate charge would be delivered then removed through the capacitor and the net charge passing through C_C would be zero.

The same concept can be applied for steady state operation to determine the DC voltage across the coupling capacitor with R_{GS} in the circuit. Assuming no clamp circuitry, a constant V_C voltage across the capacitor, and a constant duty cycle D, the current of R_{GS} can be represented as an additional charge component passing through C_C.

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Accordingly, the total charge delivered through the coupling capacitor during turn-on and consecutive on-time of the MOSFET is shown in Equation 33.

$$Q_{C,ON} = Q_G + \frac{V_{DRV} - V_C}{R_{GS}} \times \frac{D}{f_{DRV}} \tag{33}$$

Following the same considerations for the turnoff and successive off-time of the switch, the total charge can be calculated as shown in Equation 34.

$$Q_{C,OFF} = Q_G + \frac{V_C}{R_{GS}} \times \frac{1-D}{f_{DRV}} \tag{34}$$

For steady state operation, the two charges must be equal.

Solving the equations for V_C determines the voltage across the coupling capacitor.

$$V_C = V_{DRV} \times D \tag{35}$$

This well-known relationship highlights the duty ratio dependency of the coupling capacitor voltage. As duty cycle varies, V_C is changing and the turn-on and turn-off voltages of the MOSFET adjust accordingly. As Figure 32 exemplifies, at low duty cycles the negative bias during turn-off is reduced, while at large duty ratios the turn-on voltage becomes insufficient.

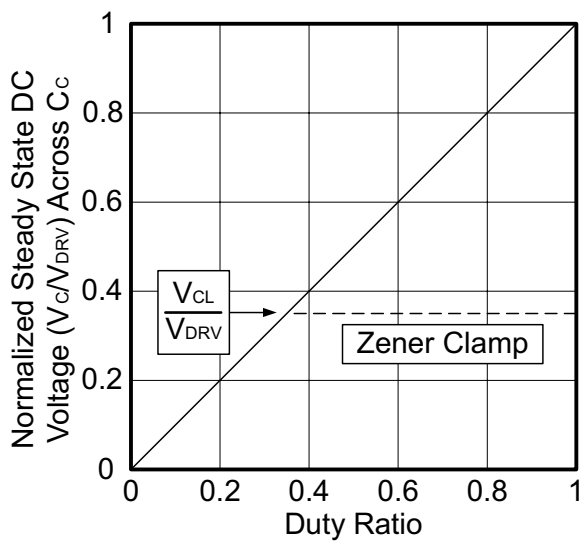

Figure 32. Normalized Coupling Capacitor Voltage as a Function of Duty Ratio

The inadequate turn-on voltage at large duty ratios can be resolved by using a clamp circuit connected in parallel to R_{GS} as shown in Figure 31. Its effect on the coupling capacitor voltage is also shown in Figure 32. As the coupling capacitor voltage is limited by the clamp, the maximum negative bias voltage of the gate is determined. Since the gate drive amplitude is not effected by the AC coupling circuit, a minimum turn-on voltage can be assured for the entire duty cycle range.

6.1 Calculating the Coupling Capacitor

The amount of charge going through C_C in every switching cycle causes an AC ripple across the coupling capacitor on the switching frequency basis. Obviously, this voltage change should be kept relatively small compared to the amplitude of the drive voltage.

The ripple voltage can be calculated based on the charge defined previously as shown in Equation 36.

$$\Delta V_C = \frac{Q_G}{C_C} + \frac{(V_{DRV} - V_C) \times D}{C_C \times R_{GS} \times f_{DRV}} \tag{36}$$

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Taking into account that $V_C = D \cdot V_{DRV}$, Equation 37 can be rearranged to yield the desired capacitor value as well.

$$C_C = \frac{Q_G}{\Delta V_C} + \frac{V_{DRV} \times (1 - D) \times D}{\Delta V_C \times R_{GS} \times f_{DRV}} \tag{37}$$

The expression reveals a maximum at D = 0.5. A good rule of thumb is to limit the worst case AC ripple amplitude (ΔV_C) to approximately 10% of V_{DRV}.

6.2 Start-Up Transient of the Coupling Capacitor

Before the desired minimum coupling capacitor value could be calculated, one more parameter must be defined. The value of R_{GS} has to be selected. In order to make an intelligent decision the start up transient of the AC coupling circuit must be examined.

At power up, the initial voltage across C_C is zero. As the output of the driver start switching the DC voltage across the coupling capacitor builds up gradually until it reaches its steady state value, V_C. The duration to develop V_C across C_C depends on the time constant defined by C_C and R_{GS}. Therefore, to achieve a target start-up transient time and a certain ripple voltage of the coupling capacitor at the same time, the two parameters must be calculated together. Fortunately, there are two equations for two unknowns:

$$C_C = \frac{Q_G}{\Delta V_C} + \frac{V_{DRV} \times (1 - D) \times D}{\Delta V_C \times R_{GS} \times f_{DRV}}$$

$$\tau = R_{GS} \times C_C \rightarrow R_{GS} = \frac{\tau}{C_C} \tag{38}$$

which yields a single solution. Substituting the expression for R_{GS} from the second equation, D = 0.5 for worst case condition and targeting $\Delta V_C = 0.1 \times V_{DRV}$, the first equation can be solved and simplified for a minimum capacitor value as shown in Equation 39.

$$C_{C,MIN} = \frac{20 \times Q_G \times \tau \times f_{DRV}}{V_{DRV} \times (2 \times \tau \times f_{DRV} - 5)} \tag{39}$$

Once $C_{C,MIN}$ is calculated, its value and the desired start-up time constant (τ) defines the required pull down resistance. A typical design trade-off for AC coupled drives is to balance efficiency and transient time constant. For quicker adjustment of the coupling capacitor voltage under varying duty ratios, higher current must be allowed in the gate-to-source resistor.

7 Transformer-Coupled Gate Drives

Before the appearance of high voltage gate drive ICs, using a gate drive transformer was the only viable solution to drive high side switches in offline or similar high voltage circuits. The two solutions coexist today, both have their pros and cons serving different applications. The integrated high side drivers are convenient, use smaller circuit board area but have significant turn-on and turn-off delays. The properly designed transformer coupled solution has negligible delays and it can operate across higher potential differences. Usually it takes more components and requires the design of a transformer or at least the understanding of its operation and specification.

Before concentrating on the gate drive circuits, some common issues pertinent to all transformer designs and their correlation to gate drive transformers will be reviewed.

- Transformers have at least two windings. The use of separate primary and secondary windings facilitates isolation. The turns ratio between primary and secondary allows voltage scaling. In the gate drive transformer, voltage scaling is usually not required, but isolation is an important feature.

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- Ideally the transformer stores no energy, there is no exemption. The so called flyback “transformer” really is coupled inductors. Nevertheless, small amounts of energy are stored in real transformers in the nonmagnetic regions between the windings and in small air gaps where the core halves come together. This energy storage is represented by the leakage and magnetizing inductance. In power transformers, reducing the leakage inductance is important to minimize energy storage thus to maintain high efficiency. The gate drive transformer handles very low average power, but it delivers high peak currents at turn-on and turn-off. To avoid time delays in the gate drive path, low leakage inductance is still imperative.
- Faraday’s law requires that the average voltage across the transformer winding must be zero over a period of time. Even a small DC component can cause flux “walk” and eventual core saturation. This rule will have a substantial impact on the design of transformer coupled gate drives controlled by single ended PWM circuits.
- Core saturation limits the applied volt-second product across the windings. The transformer design must anticipate the maximum voltsecond product under all operating conditions, which must include worst case transients with maximum duty ratio and maximum input voltage at the same time. The only relaxation for gate drive transformer design is their regulated supply voltage.
- A significant portion of the switching period might be reserved to reset the core of the main power transformer in single ended applications, (working only in the first quadrant of the B-H plane) such as the forward converter. The reset time interval limits the operating duty ratio of the transformer. This is rarely an issue even in single ended gate drive transformer designs because they must be AC coupled, thus, they operate with bi-directional magnetization.

7.1 Single-Ended Transformer-Coupled Gate-Drive Circuits

These gate drive circuits are used in conjunction with a single output PWM controller to drive a high side switch. Figure 33 shows the basic circuit.

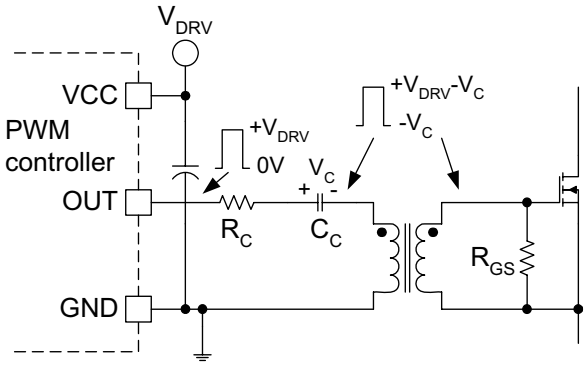

Figure 33. Single-Ended Transformer-Coupled Gate Drive

The coupling capacitor must be placed in series with the primary winding of the gate drive transformer to provide the reset voltage for the magnetizing inductance. Without the capacitor there would be a duty ratio dependent DC voltage across the winding and the transformer would saturate.

The DC voltage (V_C) of C_C develops the same way as shown in AC coupled direct drives. The steady state value of the coupling capacitor voltage is shown in Equation 40.

$$V_C = D \times V_{DRV} \tag{40}$$

Similar to AC coupled direct drives, the actual gate drive voltage, V_C, changes with duty ratio. In addition, sudden changes in duty ratio will excite the L-C resonant tank formed by the magnetizing inductance of the gate drive transformer and the coupling capacitor. In most cases, this L-C resonance can be damped by inserting a low value resistor (R_C) in series with C_C. The value of R_C is determined by the characteristic impedance of the resonant circuit and given as shown in Equation 41.

$$R_C \geq 2 \times \sqrt{\frac{L_M}{C_C}} \tag{41}$$

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Keep in mind that the R_C value defined in Equation 41 is the equivalent series resistance that includes the output impedance of the PWM driver. Additionally, consider that a critically damped response in the coupling capacitor voltage might require unreasonable high resistor value. This would limit the gate current, consequently the switching speed of the main switch. On the other hand, underdamped response may result in unacceptable voltage stress across the gate source terminals during the resonance.

The current building V_C has two components: the magnetizing current of the transformer and the current flowing in the pull down resistor connected between the gate and the source of the main MOSFET. Accordingly, the start-up and transient time constant governing the adjust speed of the coupling capacitor voltage reflects the effect of the magnetizing inductance of the gate drive transformer and can be estimated by:

$$\tau = \frac{2 \times \pi \times f_{DRV} \times L_M \times R_{GS} \times C_C}{2 \times \pi \times f_{DRV} \times L_M + R_{GS}} \tag{42}$$

The magnetizing inductance has another significant effect on the net current of the driver, and on its direction. Figure 34 highlights the different current components flowing in the circuit and the sum of the current components, I_{OUT}, which has to be provided by the driver.

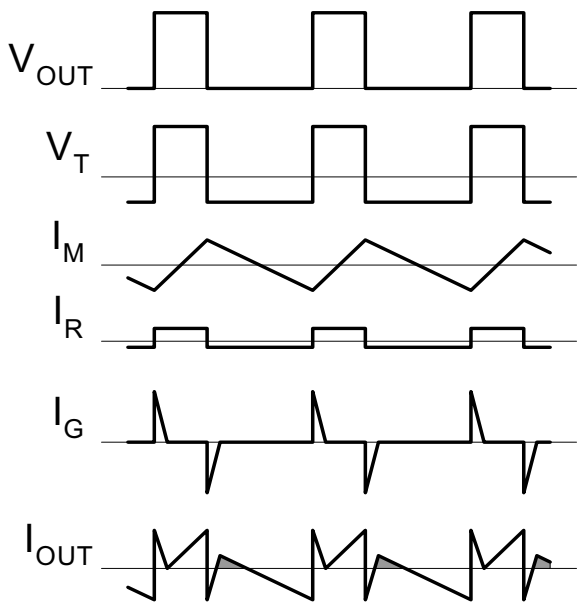

Figure 34. Driver Output Current With Transformer-Coupled Gate Drive

Note the gray shaded area in the output current waveform. The output driver is in its low state, which means it is supposed to sink current. But because of the magnetizing current component, the driver actually sources current. Therefore, the output must handle bi-directional current with transformer coupled gate drives. This might require additional diodes if the driver is not capable of carrying current in both directions. Bipolar MOSFET drivers are a typical example where a Schottky diode has to be connected between the ground and the output pin. Similar situation can occur during the high state of the driver at different duty cycle or current component values. One easy remedy to solve this problem and avoid the diodes on the driver's output is to increase the resistive current component to offset the effect of the magnetizing current.

At wide duty cycles, like in the buck converter, the circuit of Figure 33 does not provide adequate gate drive voltage. The coupling capacitor voltage increases proportionally to the duty ratio. Accordingly, the negative bias during off-time increases as well and the turn-on voltage decreases. Adding two small components on the secondary side of the gate drive transformer can prevent this situation.

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Figure 35 shows a commonly used technique to restore the original voltage levels of the gate drive pulse.

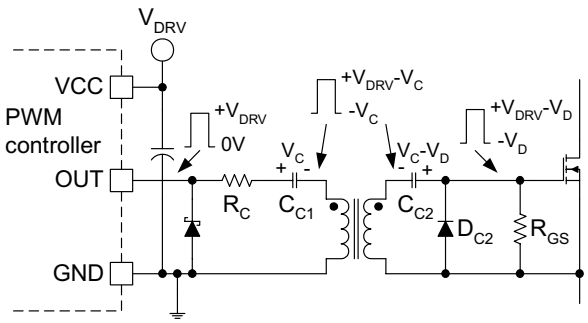

Figure 35. DC Restore Circuit in Transformer-Coupled Gate Drive

Here, a second coupling capacitor (C_{C2}) and a simple diode clamp (D_{C2}) are used to restore the original gate drive amplitude on the secondary side of the transformer. If a larger negative bias is desired during the off time of the main switch, a Zener diode can be added in series with the diode in a similar fashion as it is shown in Figure 31, with respect to the AC coupled direct drive solution.

7.1.1 Calculating the Coupling Capacitors

The method to calculate the coupling capacitor values is based on the maximum allowable ripple voltage and the amount of charge passing through the capacitor in steady state operation was described in the previous AC coupled circuits. The equation for C_{C2} is similar to the one identified for direct coupled gate drive circuit. The ripple has two components: one is related to the total gate charge of the main MOSFET and a second component due to the current flowing in the gate pull down resistor:

$$C_{C2} = \frac{Q_G}{\Delta V_{C2}} + \frac{\left(V_{DRC} - V_{DC2,FW}\right) \times D_{MAX}}{\Delta V_{C2} \times R_{GS} \times f_{DRV}} \tag{43}$$

This expression has a maximum at the maximum on-time of the switch, that is, at maximum duty ratio. In the primary side coupling capacitor the magnetizing current of the gate drive transformer generates an additional ripple component. Its effect is reflected in Equation 44 that can be used to calculate the primary side coupling capacitor value.

$$C_{C1} = \frac{Q_G}{\Delta V_{C1}} + \frac{(V_{DRV} - V_{DC2,FW}) \times D}{\Delta V_{C1} \times R_{GS} \times f_{DRV}} + \frac{V_{DRV} \times (D^2 - D^3)}{\Delta V_{C1} \times 4 \times L_M \times f_{DRV}^2} \tag{44}$$

The minimum capacitance assured to stay below the targeted ripple voltage under all operating conditions can be found by determining the maximum of the above expression. Unfortunately, the maximum occurs at different duty ratios depending on the actual design parameters and component values. In the majority of practical solutions, it falls between D = 0.6 and D = 0.8 range.

Also note that the sum of the ripple voltages, $\Delta V_{C1} + \Delta V_{C2}$ appears at the gate terminal of the main MOSFET transistor. When aiming for a particular ripple voltage or droop at the gate terminal, it has to be split between the two coupling capacitors.

7.1.2 Gate-Drive Transformer Design

The function of the gate drive transformer is to transmit the ground referenced gate drive pulse across large potential differences to accommodate floating drive implementations. Like all transformers, it can be used to incorporate voltage scaling, although it is rarely required. It handles low power but high peak currents to drive the gate of a power MOSFET. The gate drive transformer is driven by a variable pulse width as a function of the PWM duty ratio and either constant or variable amplitude depending on the circuit configuration. In the single ended circuits the gate drive transformer is AC coupled and the magnetizing inductance sees a variable amplitude pulse. The double ended arrangements, such as half-bridge applications, drive the gate drive transformer with a constant amplitude signal. In all cases, the gate drive transformers are operated in both, the first and third quadrant of the B-H plane.

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The gate drive transformer design is very similar to a power transformer design. The turns ratio is usually one, and the temperature rise due to power dissipation is usually negligible. Accordingly, the design can be started with the core selection. Typical core shapes for gate drive transformer include toroidal , RM, P or similar cores. The core material is high permeability ferrite to maximize the magnetizing inductance value, consequently lower the magnetizing current. Seasoned designers can pick the core size from experience or it can be determined based on the area product estimation in the same way as it is required in power transformer design. Once the core is selected, the number of turns of the primary winding can be calculated by Equation 45.

$$N_P = \frac{V_{TR} \times t}{\Delta B \times A_e}$$

where

- V_{TR} is the voltage across the primary winding
- t is the duration of the pulse
- ΔB is the peak-to-peak flux change during t
- A_e is the equivalent cross section of the selected core (45)

The first task is to find the maximum volt-second product in the numerator. Figure 36 shows the normalized volt-second product for both single ended and double ended gate drive transformers as the function of the converter duty cycle.

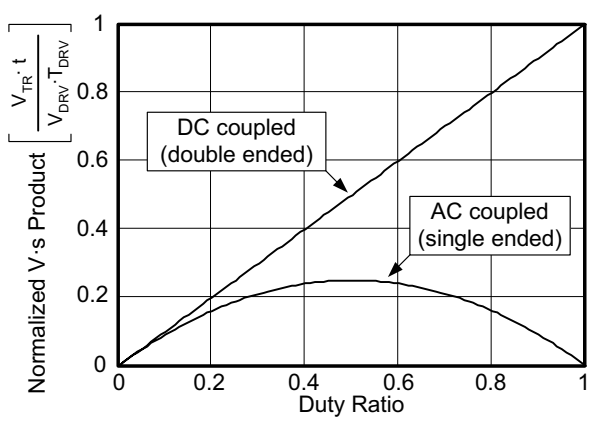

Figure 36. Gate-Drive Transformer Volt-second Product vs. Duty Ratio

For an AC coupled circuit, the worst case is at D = 0.5 while direct coupling reaches the peak volt-second value at the maximum operating duty ratio. Interestingly, the AC coupling reduces the maximum steady state volt-second product by a factor of four because at large duty ratios the transformer voltage is proportionally reduced due to the voltage developing across the coupling capacitor.

It is much more difficult to figure out ΔB in the Np equation. The reason is flux walking during transient operation. When the input voltage or the load are changing rapidly, the duty ratio is adjusted accordingly by the PWM controller. Deducing exact quantitative result for the flux walk is rather difficult. It depends on the control loop response and the time constant of the coupling network when it is present. Generally, slower loop response and a faster time constant have a tendency to reduce flux walking. A three to one margin between saturation flux density and peak flux value under worst case steady state operation is desirable for most designs to cover transient operation.

The next step is to arrange the windings in the available window area of the core. As mentioned before, the leakage inductance should be minimized to avoid time delay across the transformer, and the AC wire resistance must be kept under control. On toroidal cores, the windings should be wound bifilar or trifilar depending on the number of windings in the gate drive transformer. With pot cores, each winding should be kept in a single layer. The primary should be the closest to the center post, followed by the low side winding, if used, and the high side winding should be the farthest from the center post. This arrangement in pot cores provides an acceptable leakage inductance and the lowest AC winding resistance. Furthermore, natural shielding of the control (primary) winding against capacitive currents flowing between the floating components and power ground is provided by the low side winding, which is usually connected to the power ground directly.

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7.1.3 Dual-Duty Transformer-Coupled Circuits

There are high side switching applications where the low output impedance and short propagation delays of a high speed gate drive IC are essential. Figure 37 and Figure 38 show two fundamentally different solutions to provide power as well as control to regular low voltage gate drive ICs in a floating application using only one transformer.

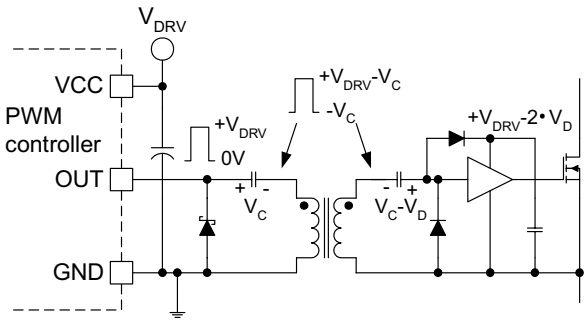

Figure 37. Power and Control Transmission With One Transformer

The circuit of Figure 37 uses the switching frequency to carry the control signal and the power for the driver. The operation is rather simple. During the on-time of the main switch, the positive voltage on the secondary side of the transformer is peak rectified to generate the supply voltage for the gate drive IC. Since the power is generated from the gate drive pulses, the first few drive pulses must charge the bias capacitor. Therefore, it is desirable that the driver IC chosen for this application has an under voltage lock out feature to avoid operation with insufficient gate voltage. As it is shown in the circuit diagram, the DC restoration circuit (C_{C2} and D_{C2}) must be used to generate a bias voltage for the driver, which is independent of the operating duty ratio. D_{C2} also protects the input of the driver against the negative reset voltage of the transformer secondary winding. The transformer design for this circuit is basically identical to any other gate drive transformer design. The power level is just slightly increased by the power consumption of the driver IC, which is relatively small compared to the power loss associated by the total gate charge of the MOSFET. The transformer carries a high peak current but this current charges the bypass capacitor, not the input capacitance of the MOSFET. All gate current is contained locally between the main transistor, driver IC and bypass capacitor.

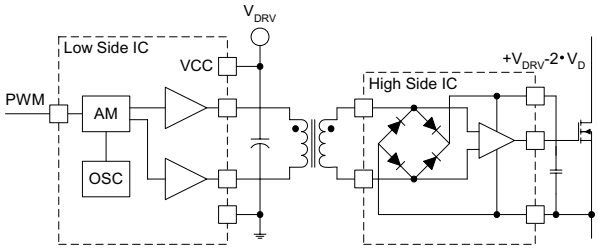

Figure 38. Power and Control Transmission With One Transformer

Another similar solution to transfer power and control signal with the same transformer is shown in Figure 38. The difference between the two circuits in Figure 37 and Figure 38 is the operating frequency of the transformer. This implementation utilizes a dedicated chip pair. The high frequency carrier signal ($f_{CARRIER} >> f_{DRV}$) is used to power transfer, while amplitude modulation transmits the control command. The basic blocks of the gate drive schematic in Figure 38 can be integrated into two integrated circuits allowing efficient utilization of circuit board area. Because of the high frequency operation, the transformer size can be reduced compared to traditional gate drive transformers. Another benefit of this solution is that the bias voltage of the floating driver can be established independently of the gate drive commands, thus the driver can react without the start-up delay discussed in the previous solution.

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7.2 Double-Ended Transformer-Coupled Gate Drives

In high power half-bridge and full-bridge converters, the need arises to drive two or more MOSFETs usually controlled by a push-pull or also called double-ended PWM controller. A simplified schematic of such gate drive circuit is illustrated in Figure 39.

In these applications a dual polarity symmetrical gate drive voltage is readily available. In the first clock cycle, OUTA is on, forcing a positive voltage across the primary winding of the gate drive transformer. In the next clock cycle, OUTB is on for the same amount of time (steady state operation) providing an opposite polarity voltage across the magnetizing inductance. Averaging the voltage across the primary for any two consecutive switching period results zero volts.

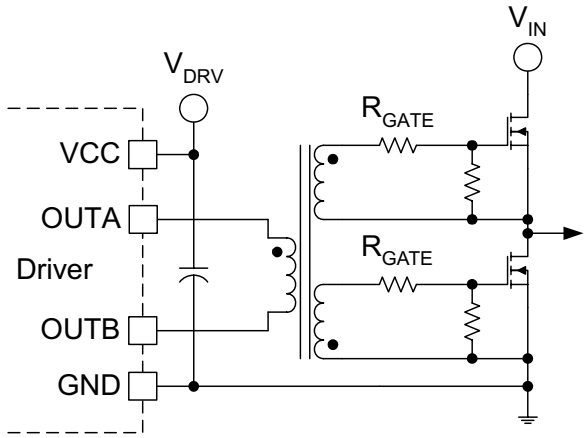

Figure 39. Push-Pull Type Half-Bridge Gate Drive

Therefore, AC coupling is not needed in pushpull type gate drive circuits.

Designers are often worried about any small amount of asymmetry that could be caused by component tolerances and offsets in the controller. These small deviations are easily compensated by the output impedance of the driver or by a small resistor in series with the primary winding of the transformer. The uneven duty cycle causes a small DC current in the transformer, which generates a balancing voltage across the equivalent resistance of the drive circuit. Assuming two different duty ratios, D_A and D_B for the PWM outputs, the DC current level of the magnetizing inductance is defined as shown in Equation 46.

$$I_{DC} = \frac{V_{DRV}}{2 \times R_{EQV}} \times (D_A - D_B) \tag{46}$$

To demonstrate the triviality of this problem, assume that D_A = 0.33, D_B = 0.31 (6% relative duty ratio difference!), V^{DRV} = 12 V, and R_{EQV} = 5Ω, which is the sum of one low side and one high side driver output impedance. The resulting D_C current is 24 mA and the excess power dissipation is only 3 mW.

The design of the gate drive transformer follows the same rules and procedures as already described in this section. The maximum voltsecond product is defined by V_{DRV} and the switching period, because push-pull circuits are usually not duty ratio limited.

Appropriate margin (approximately 3:1) between worst case peak flux density and saturation flux density must be provided.

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A unique application of the push-pull type gate drive circuits is given in Figure 40 to control four power transistors in a phase shift modulated fullbridge converter.

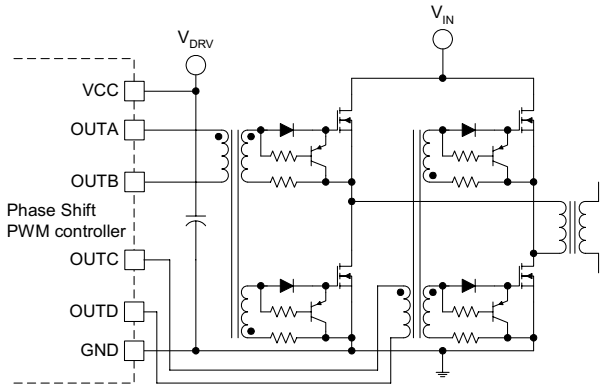

Figure 40. Push-Pull Type Half-Bridge Gate Drive

Due to the phase shift modulation technique, this power stage uses four approximately 50% duty cycle gate drive signals. The two MOSFETs in each leg requires a complementary drive waveform, which can be generated by the two output windings of the same gate drive transformer. Although, steady state duty ratios are always 0.5, changing the phase relationship between the two complementary pulse trains necessitates to have an asymmetry in the duty cycles. Therefore, during transient operation the PWM outputs are not producing the normal 50% duty cycle signals for the gate drive transformers. Accordingly, a safety margin must be built in the transformer to cover uneven duty ratios during transients.

Another interesting fact to point out is that local turn-off circuits can be easily incorporated and are very often needed on the secondary side of the transformer. The gate drive transformer, more precisely the leakage inductance of the transformer exhibits a relatively high impedance for fast changing signals. The turn-off speed and dv/dt immunity of the power circuit can be severely impacted if the driver's pull down capability is not optimized for high speed switching applications.

8 Summary

Every consideration described earlier regarding switching speeds, dv/dt immunity, bypassing rules, and so forth are equally applicable for all circuits including transformer coupled gate drives. As the topics build upon each other, only the unique and new properties of the particular circuit have been highlighted.

This application report demonstrated a systematic approach to design high performance gate drive circuits for high speed switching applications. The procedure can be summarized by the following step-by-step checklist:

- The gate drive design process begins AFTER the power stage is designed and the power components are selected.
- Collect all relevant operating parameters. Specifically, the voltage and current stresses of the power MOSFET based on the application requirements, operating junction temperature, dv/dt and di/dt limits related to external circuits around the power MOSFET that are often determined by the different snubber or resonant circuitry in the power stage.
- Estimate all device parameters that describe the parasitic component values of the power semiconductor in the actual application circuit. Data sheet values are often listed for unrealistic test conditions at room temperature and they must be corrected accordingly. These parameters include the device capacitances, total gate charge, $R_{DS(on)}$, threshold voltage, Miller plateau voltage, internal gate mesh resistance, and so forth.
- Prioritize the requirements: performance, printed circuit board size, cost target, and so forth. Then choose the appropriate gate drive circuit to match the power stage topology.
- Establish the bias voltage level that will be used to power the gate drive circuit and check for sufficient voltage to minimize the $R_{DS(on)}$ of the MOSFET.
- Select a driver IC, gate-to-source resistor value, and the series gate resistance R_{GATE} according to the targeted power-up dv/dt, and desired turn-on and turn-off switching speeds.

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- Design (or select) the gate drive transformer, if needed.
- Calculate the coupling capacitor values in case of AC coupling.
- Check start-up and transient operating conditions, especially in AC coupled gate drive circuits.
- Evaluate the dv/dt and di/dt capabilities of the driver and compare it to the values determined by the power stage.
- Add one of the turn-off circuits, if needed, and calculate its component values to meet dv/dt and di/dt requirements.
- Check the power dissipation of all components in the driver circuitry.
- Calculate the bypass capacitor values.
- Optimize the printed circuit board layout to minimize parasitic inductances.
- Always check the gate drive waveform on the final printed circuit board for excessive ringing at the gate-source terminals and at the output of the driver IC.
- Add protection or tune the resonant circuits by changing the gate drive resistor as needed.

In a reliable design, these steps should be evaluated for worst case conditions as elevated temperatures, transient voltage and current stresses can significantly change the operation of the driver, consequently the switching performance of the power MOSFET.

Of course, there are many more gate drive implementations that are not discussed in this document. Hopefully, the principles and methods presented here can help the reader's understanding and analyzing of other solutions. For those who are looking for quick answers in the rather complex field of high speed gate drive design, see Appendix A through E offer typical, numerical examples of the different calculations (Seminar 1400 Topic 2 Appendix A/F Est MOSFET Parameters from the Data Sheet). Appendix F from Seminar 1400 Topic 2 Appendix A/F Est MOSFET Parameters from the Data Sheet provides a complete, step-by-step gate drive design example for an active clamp forward converter with a ground referenced and a floating gate drive circuits.

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